LOW-POWER HIGH-SPEED ROBUST SUPPLY-GATED-SLEEP 6T SRAM CELL

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COURSE NAME : VLSI I LAB

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INTRODUCTION

SRAM means Static Random Access Memory. 6T SRAM cell consists of two crossly coupled Inverters and access transistors to read and write the data. In case of the SRAM cell the memory built is stored around the two cross coupled inverters. In this presentation, we will be presenting three types of 6T SRAM cells. These are conventional 6T SRAM, existing 6T SRAM and proposed 6T SRAM.

Conventional 6T SRAM

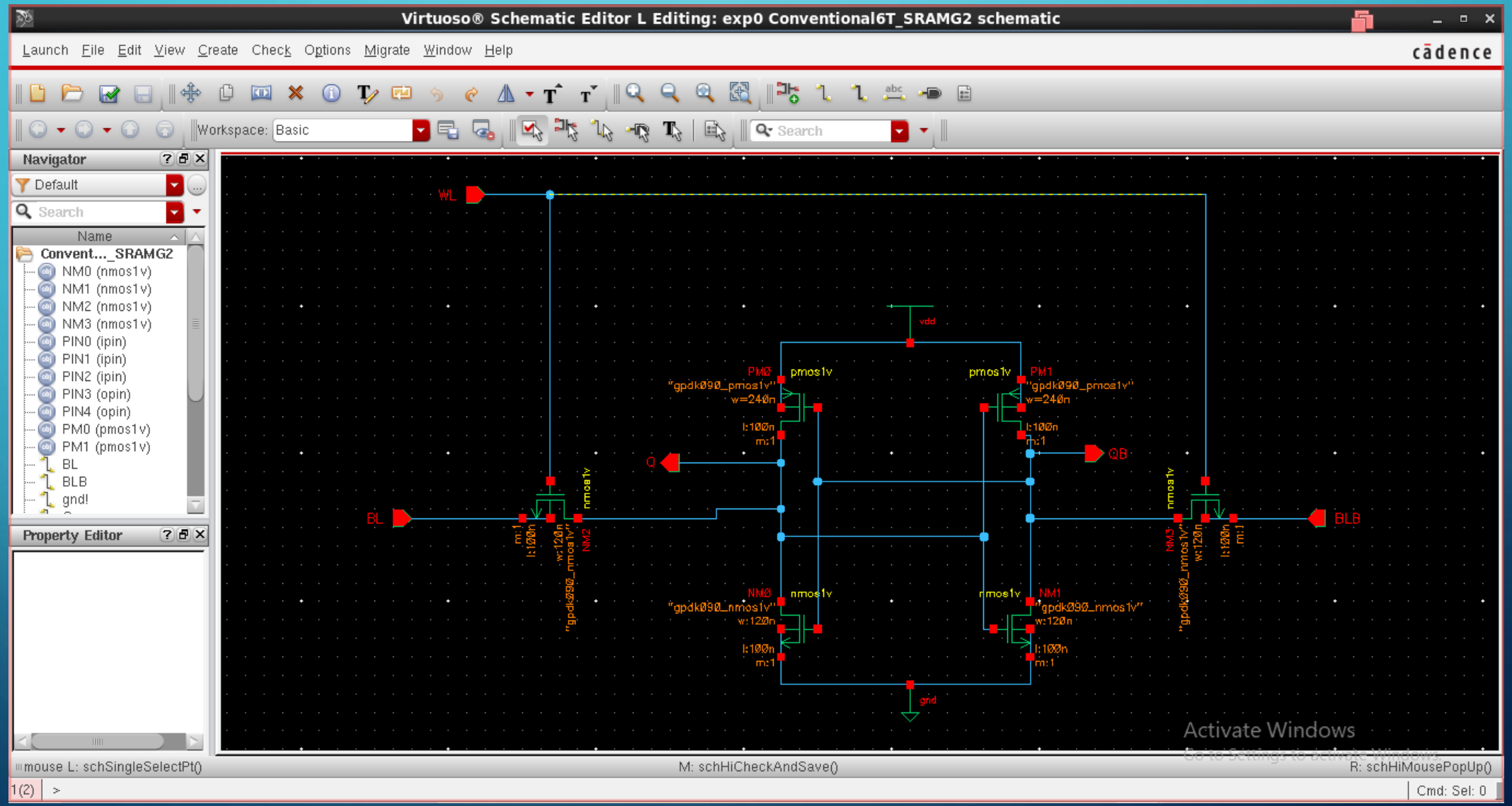
Three modes of operation

☐ Standby mode : In standby mode word line WL is zero, then the access transistors are OFF state. So the SRAM cell cannot be accessed and the contents of the cross-coupled transistors are remaining unchanged as long as supply voltage exists.

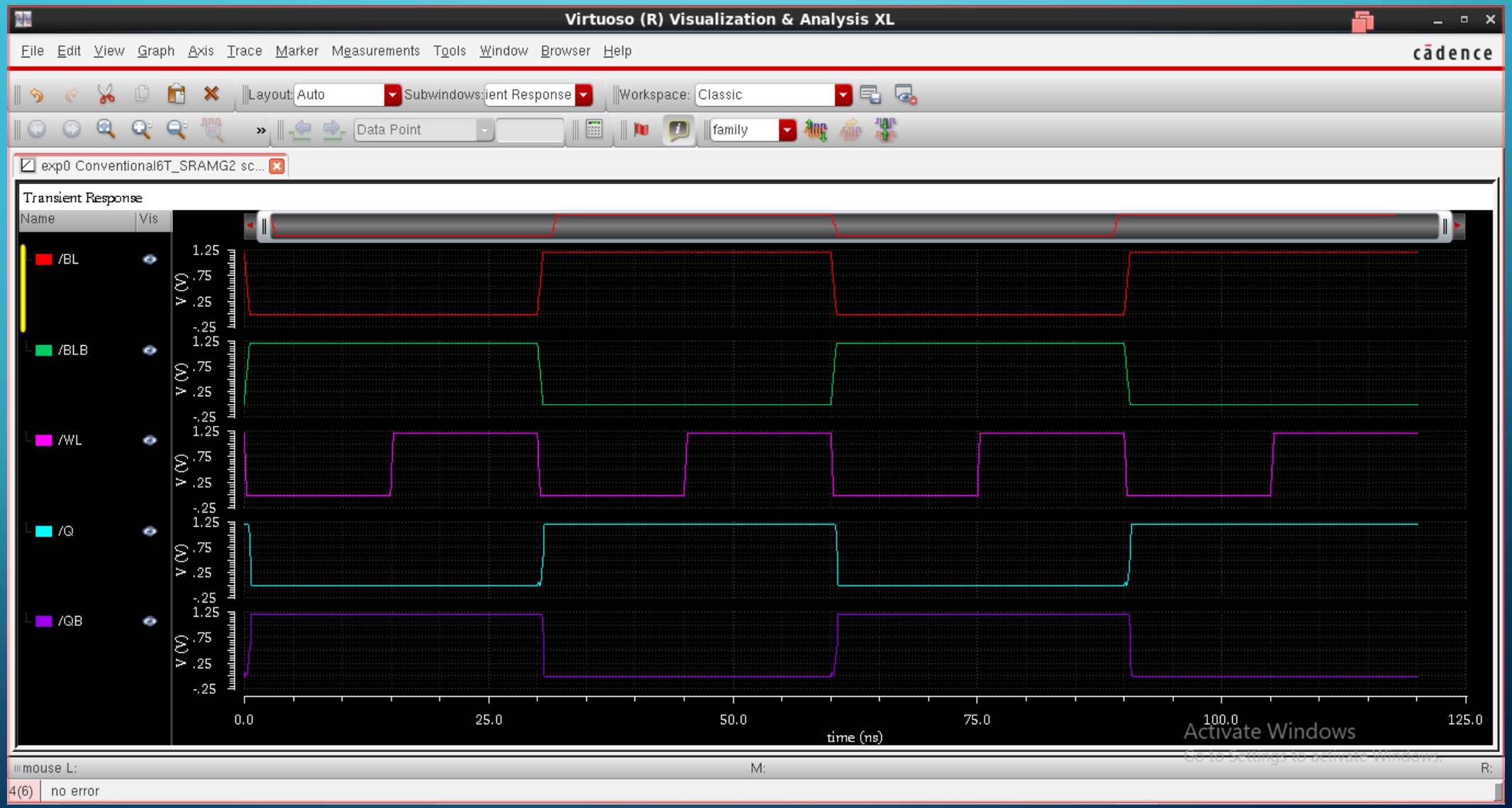
☐ Read mode : In read mode, WL gets active and it enables the two pass transistors which are connected to the bit lines. Then the value stored at node BL and BLB are transferred to the bit lines BL.

☐ Write mode : In write mode, BLB and BL is charged to Vdd and WL gets active. To written something in SRAM either BLB or BL is discharge to ground.

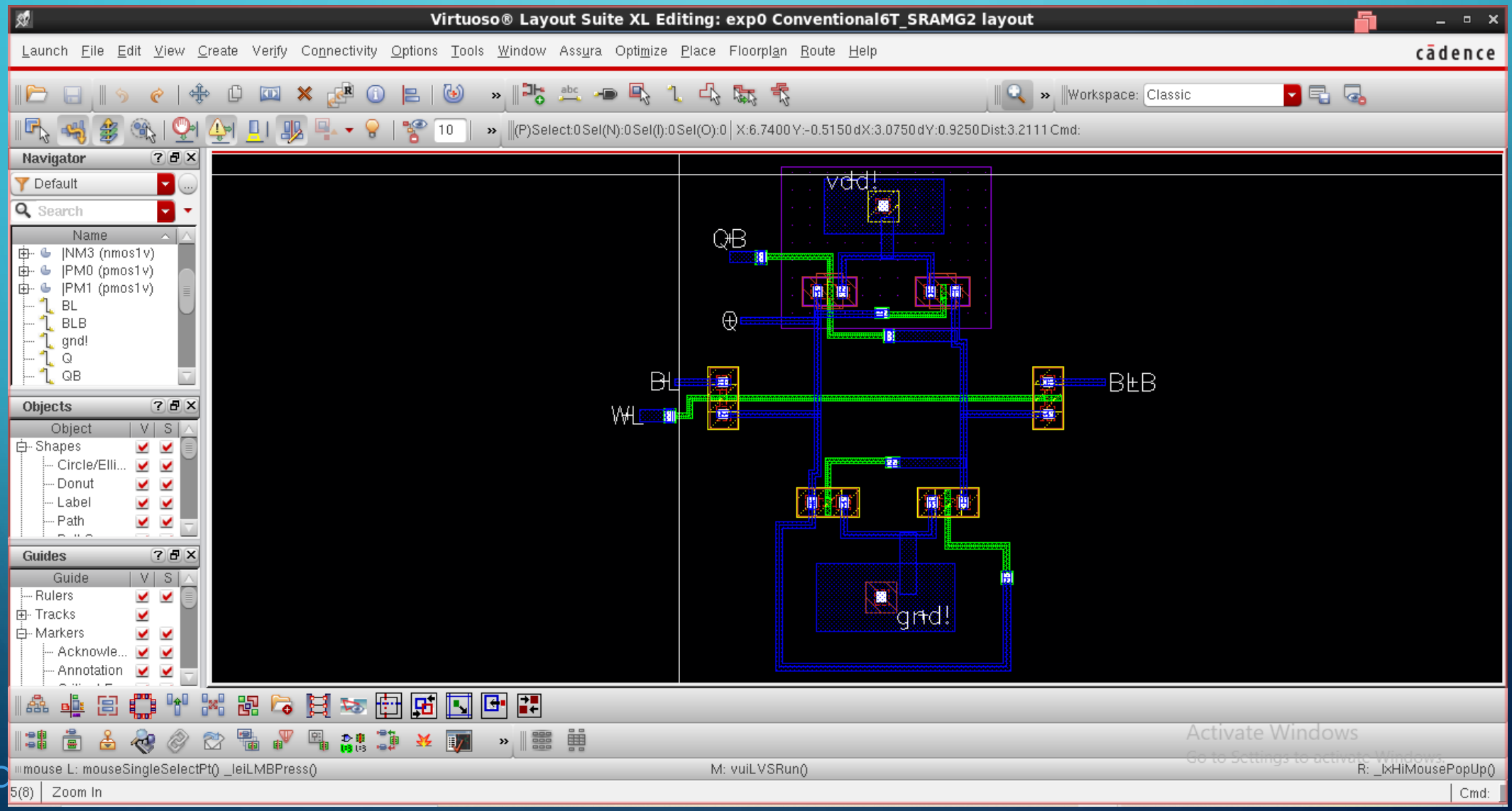
Schematic Diagram

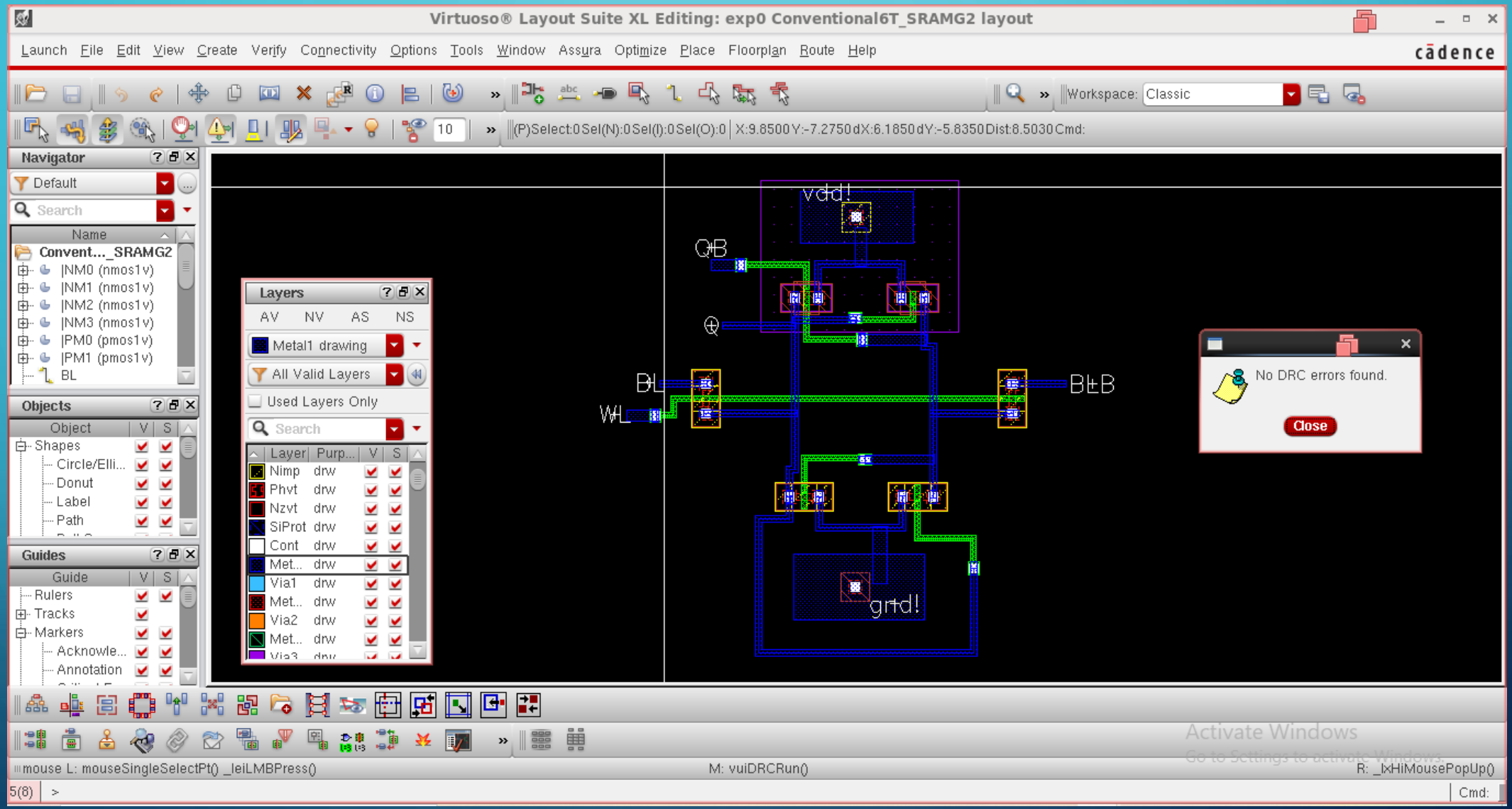


Output Waveform



Layout Diagram

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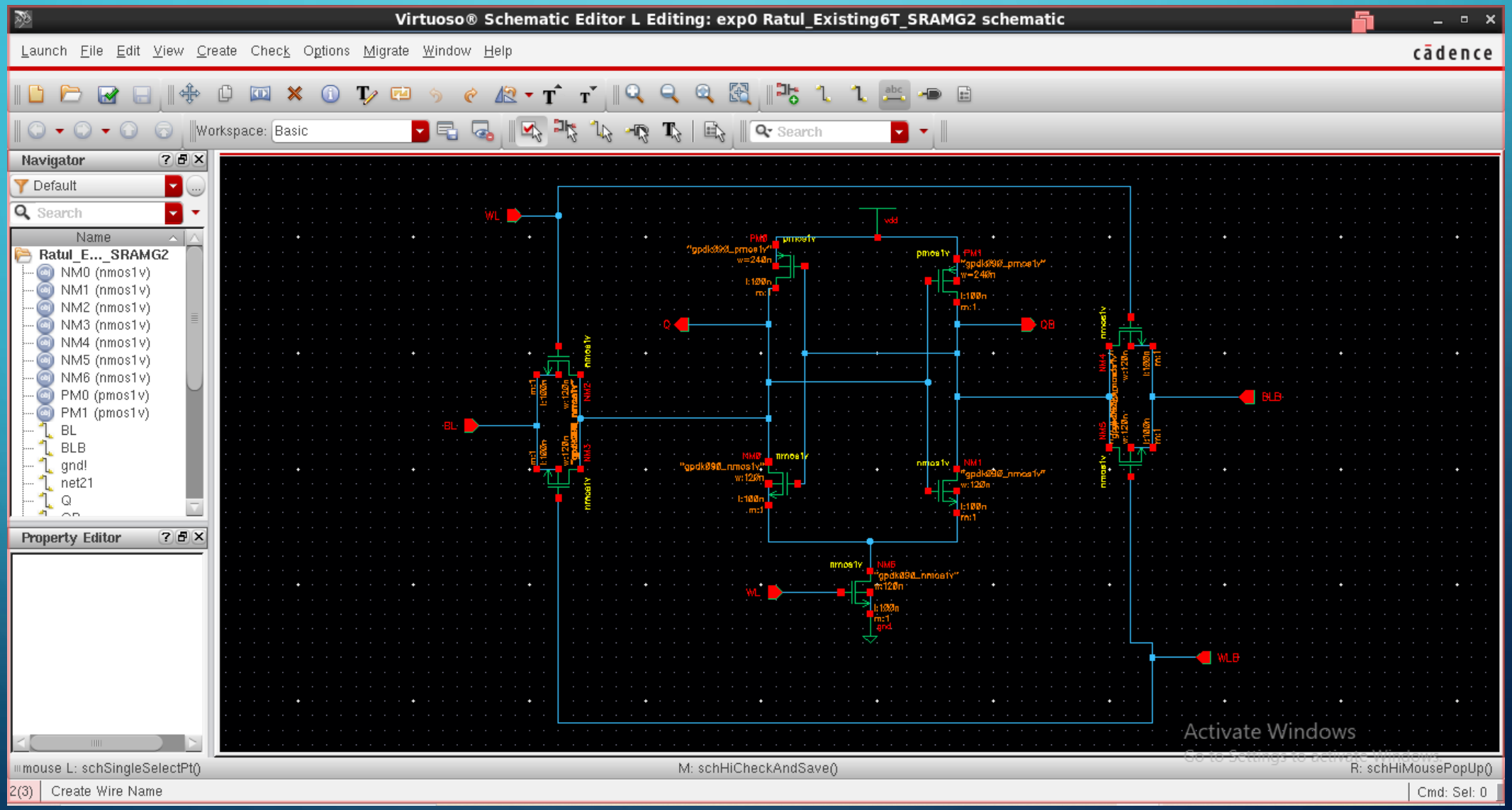
Existing 6T SRAM

Two techniques are used:

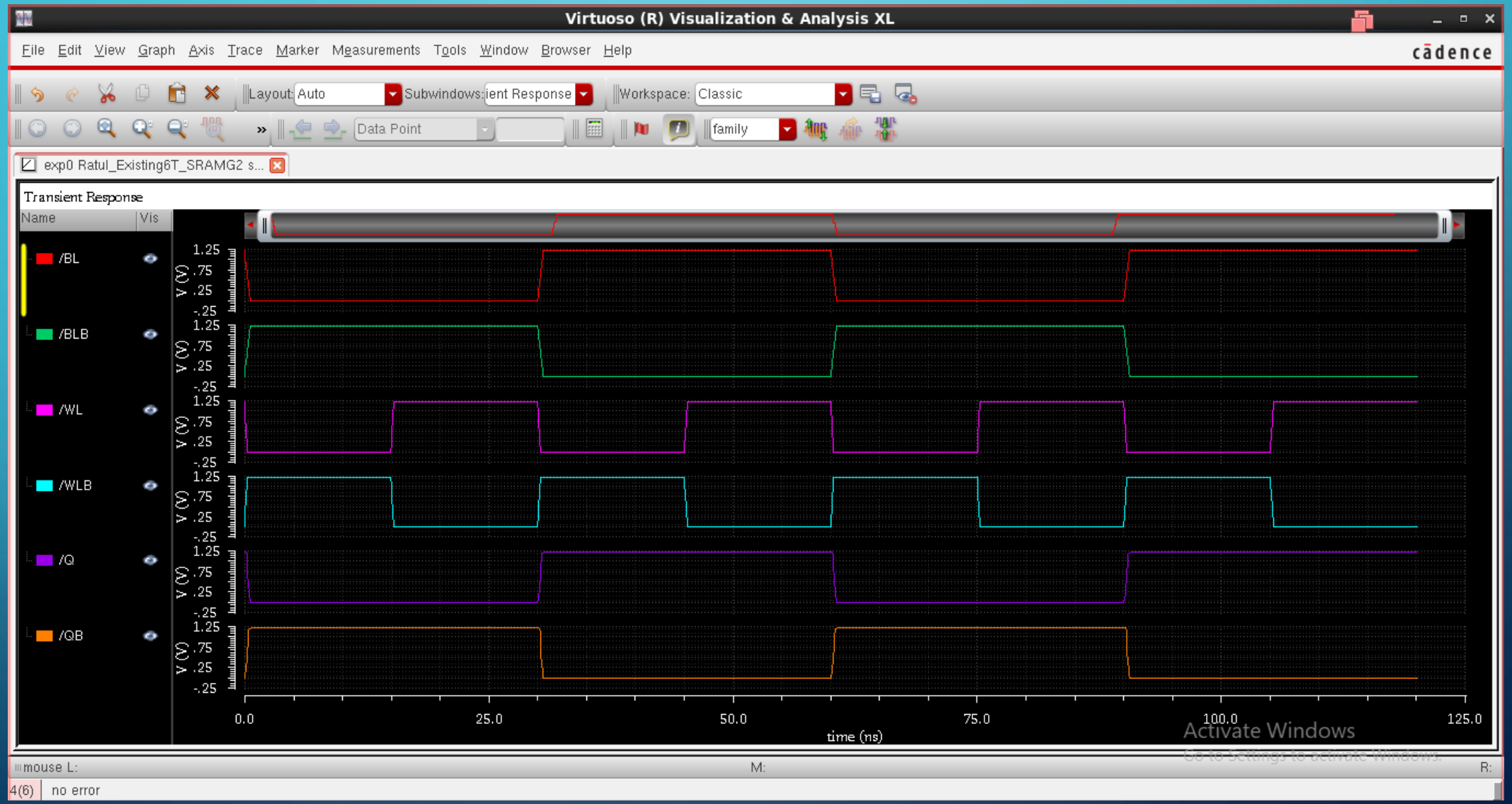
☐ Transmission gate logic : In this existing model, the transmission gates have to replace the access transistors of the conventional model. In the conventional model, the PMOS and NMOS transistors can transmit only strong 1 and strong 0 respectively and poor 0 and poor 1 respectively. This problem can be resolved with the usage of transmission gates which can transmit both 1 and 0 bits in strong.

☐ Gated ground technique : In gated ground technique, a NMOS transistor is placed between pull-down network of SRAM and ground. This extra NMOS transistor is turned OFF during the standby mode of operation. The extra transistor is turned ON, during regular mode of operation.

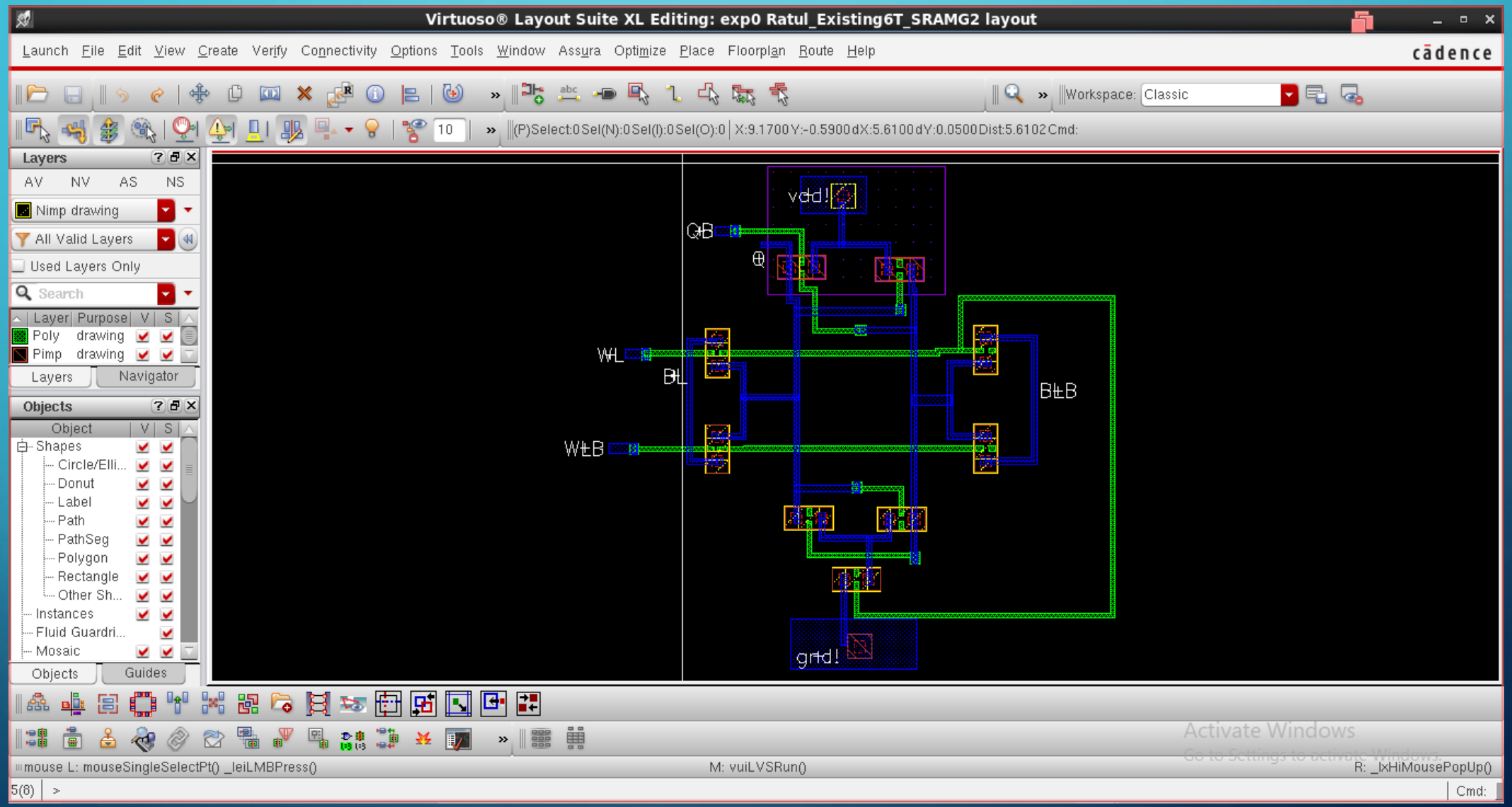
Schematic Diagram

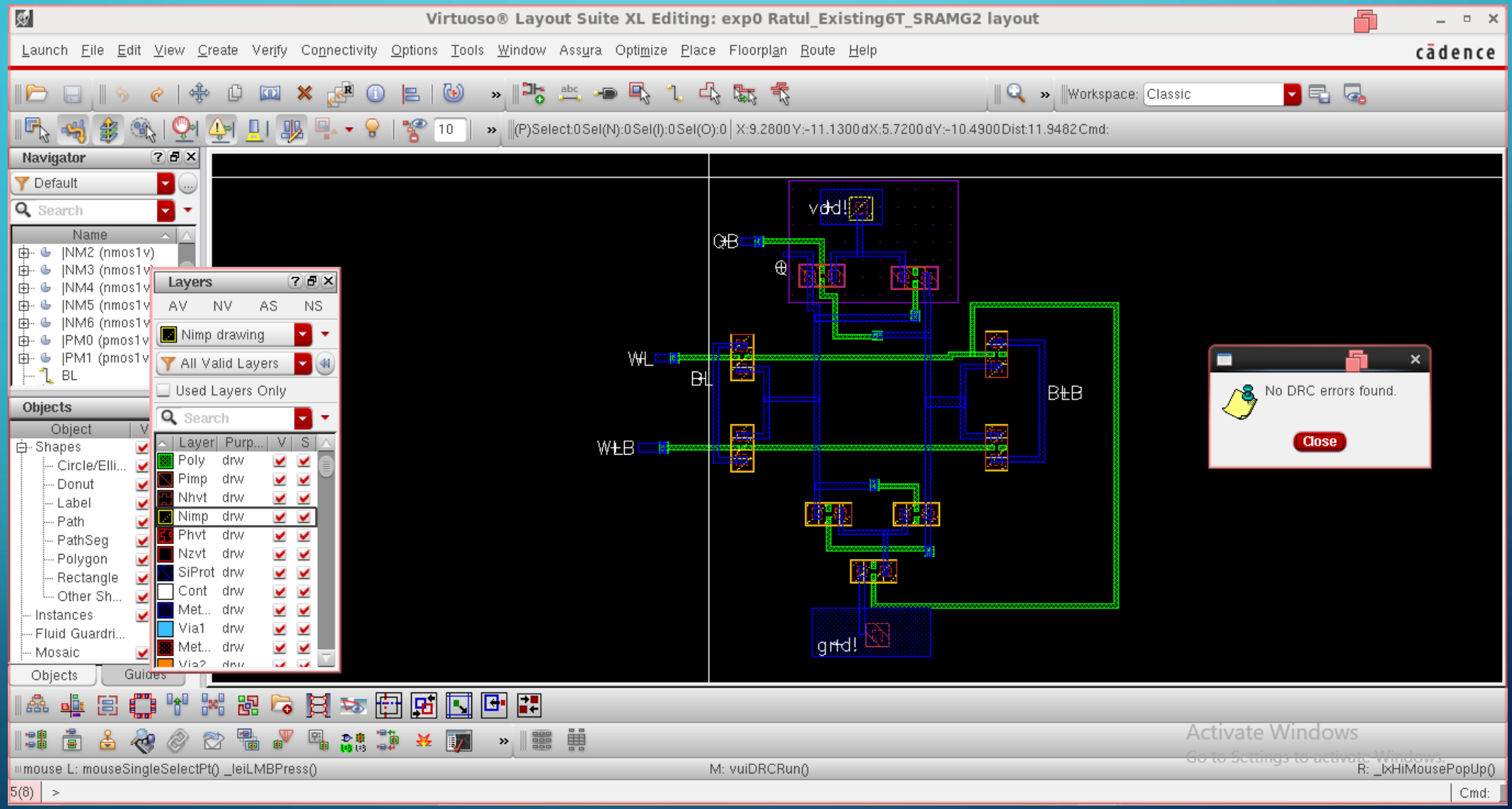


Output Waveform



Layout Diagram

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mouse L: mouseSingleSelectPt() _leiLMBPress()
M: vuiDRCRun()
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Cmd:

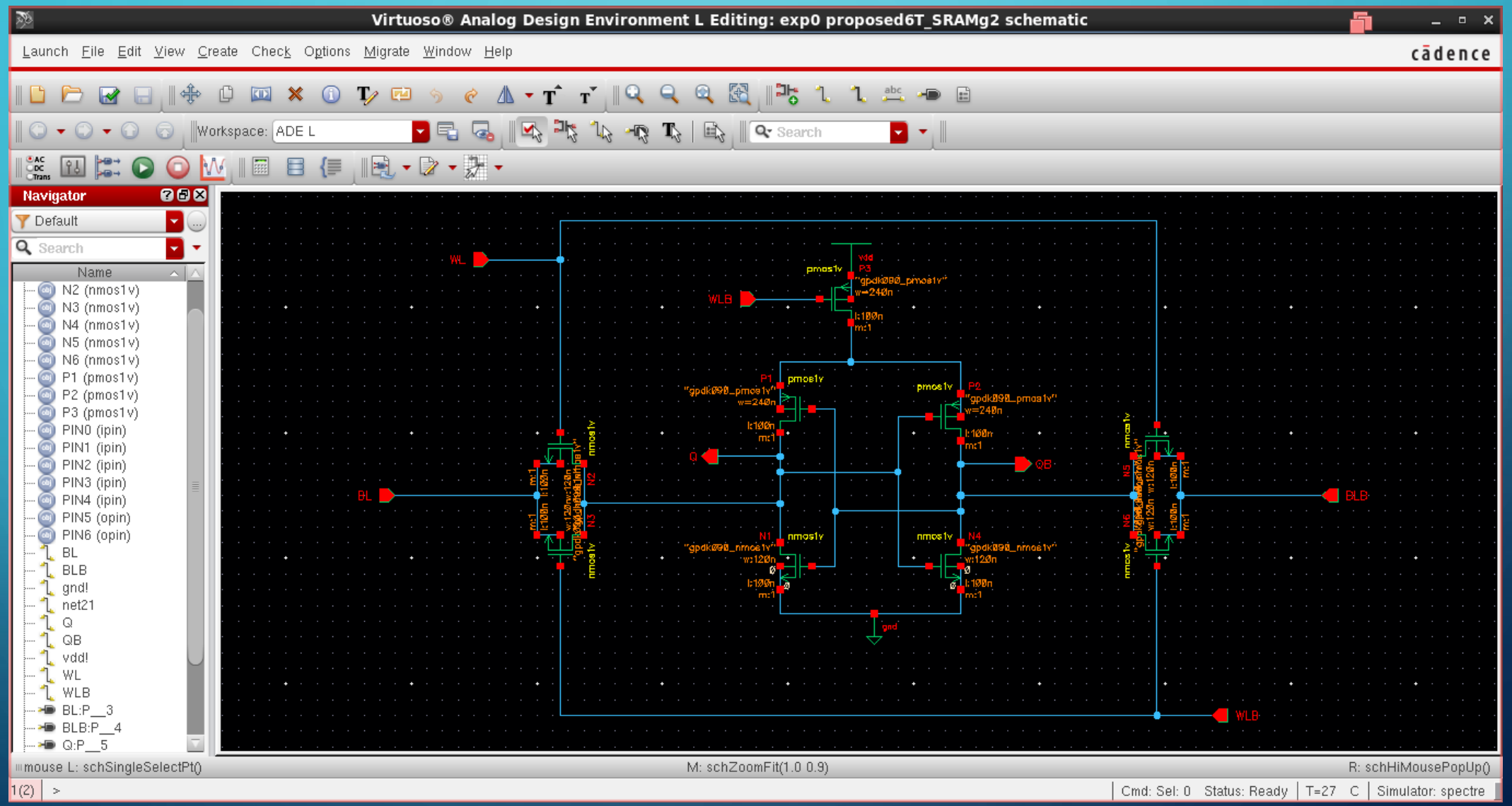
Proposed 6T SRAM

Two techniques are used:

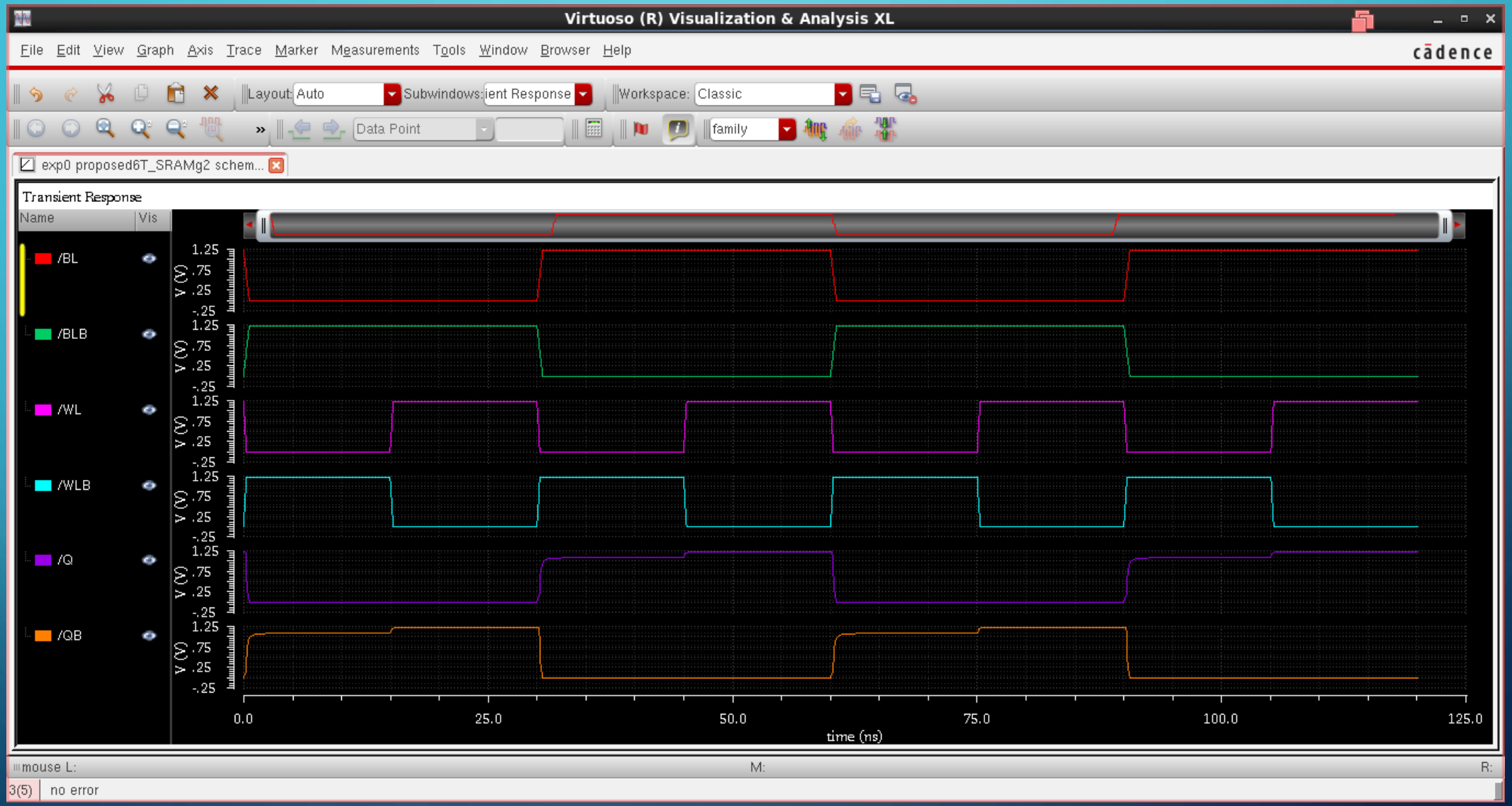
☐ Transmission gate logic : In this proposed supply gated 6T SRAM model, the transmission gates have to replace the access transistors of the conventional model.

☐ Supply gated technique : In supply gated technique, a PMOS transistor is placed between pull-up network of SRAM and the supply voltage. So the static leakage through the supply is reduced.

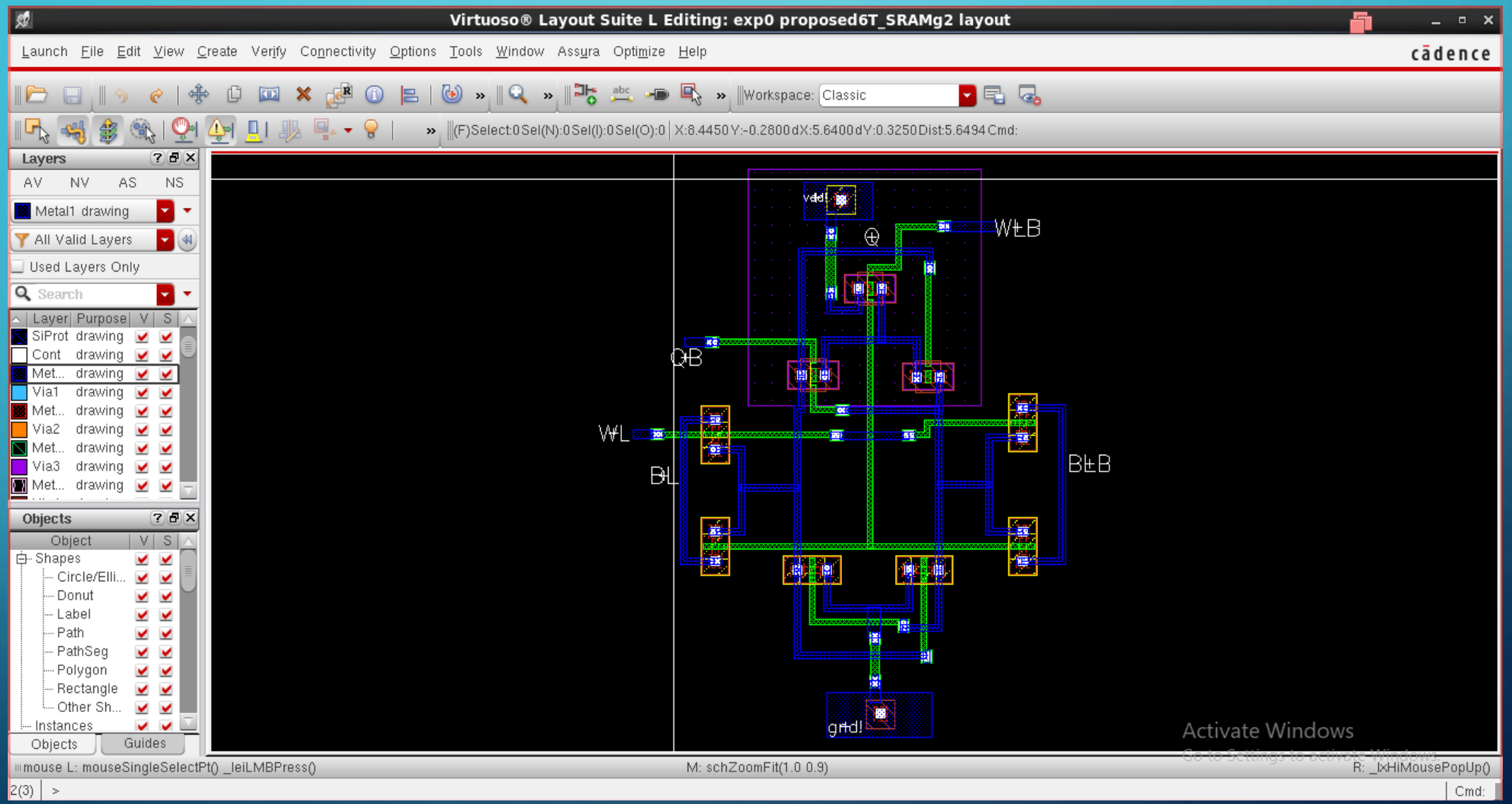
Schematic Diagram

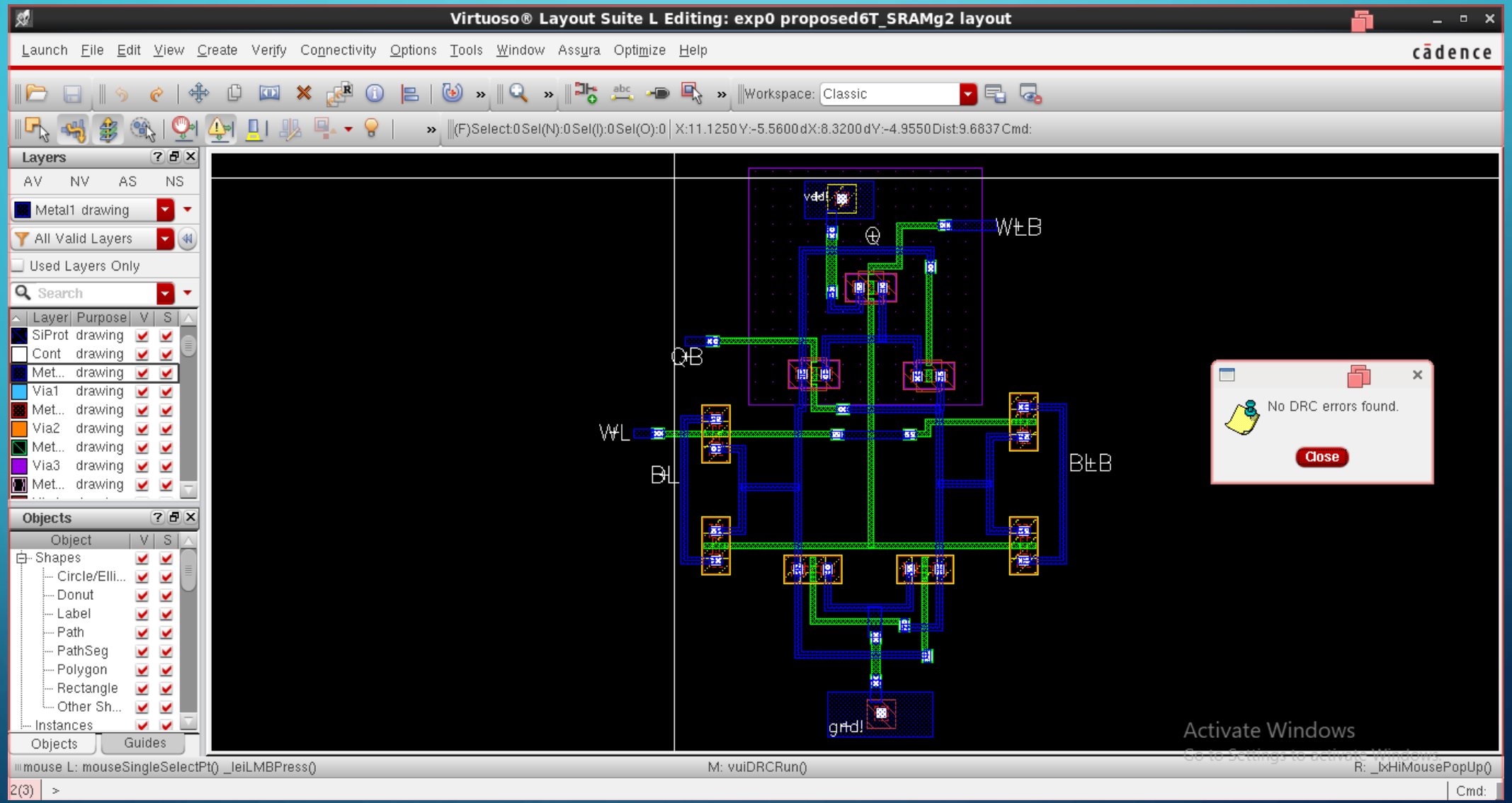


Output Waveform



Layout Diagram




Virtuoso® Layout Suite L Editing: exp0 proposed6T_SRAMg2 layout
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No DRC errors found.
Close
Activate Windows
mouse L: mouseSingleSelectPt() _leiLMBPress()
M: vuiDRCRun()
R: _lxHiMousePopUp()
2(3)
Cmd:

Result Comparison Table

Conventional 6T SRAM cell	Existing 6T SRAM cell	Proposed 6T SRAM cell
1.Sharp output waveform	1.Sharp output waveform	1.Tiny fluctuated output waveform

Conclusion

The simulation of conventional structure, existing gated ground structure and proposed gated supply structure for 6T SRAM cells has been carried out successfully with the help of Cadence Virtuoso software tool.

Thank You