Low Power SRAM design using MOSFET

A Thesis Submitted by-

Rakib Hasan Ripon ID:18.01.05.160
Khairul Islam Ratul ID:18.01.05.198
Md.Razib Hossain ID: 18.01.05.204
Samia Monjori Sazeen ID:18.01.05.207

A Thesis Submitted In Partial Fulfillment The Requirements for the Degree of Bachelor of Science in Electrical & Electronic Engineering

Supevisor
Dr.Satyendra Nath Biswas (Ph.D.,P.E)

Professor
Department of Electrical and Electronic Engineering

Department of Electrical and Electronic Engineering
Ahsanullah University of Science and Technology (AUST)

November 2022

Low Power SRAM design using MOSFET

A Thesis Submitted by-

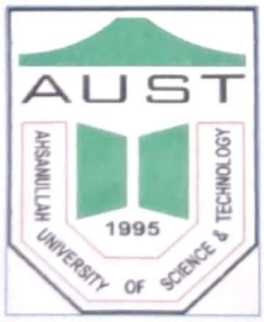
Rakib Hasan Ripon	ID:18.01.05.160
Khairul Islam Ratul	ID:18.01.05.198
Md.Razib Hossain	ID: 18.01.05.204
Samia Monjori Sazeen	ID:18.01.05.207

A Thesis Submitted In Partial Fulfillment The Requirements for the Degree of

Bachelor of Science in Electrical & Electronic Engineering

Supevisor
Dr.Satyendra Nath Biswas (Ph.D.,P.E)

Professor
Department of Electrical and Electronic
Engineering



Department of Electrical and Electronic Engineering

Ahsanullah University of Science and Technology (AUST)

November 2022

CERTIFICATION OF APPROVAL

The thesis titled "Low Power SRAM design using MOSFET " submitted by the declared students of the Department of Electrical and Electronic Engineering, Ahsanullah University of Science and Technology (AUST), Dhaka, Bangladesh, in partial fulfillment of the requirements for the BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING in November 2022 has been accepted as satisfactory.

.....

Supevisor
Dr.Satyendra Nath Biswas (Ph.D.,P.E)

Professor
Department of Electrical and Electronic

EngineeringAhsanullah University of Science and
Technology, Dhaka, Bangladesh

DECLARATION

It is hereby declared that this thesis titled "Low power SRAM design using MOSFET" has not been submitted elsewhere, partially or fully, for the award of any other degree or diploma. This thesis is a representation of the original research work and hard work done by the undersigned. It does not breach copyright law and has not been taken from other sources except where such work has been cited and acknowledged within the text.

Name: Rakib Hasan Ripon ID:18.01.05.160

Name: Khairul Islam Ratul ID:18.01.05.198

Name: Md.Razib Hossain ..... ID: 18.01.05.204

Name: Samia Monjori Sazeen ID:18.01.05.207

Acknowledgments

All praise, thanks, and glory to the Most Gracious and Most Merciful AImighty Allah (s.w.t) for giving us the strength, patience, knowledge, and capability to complete this thesis successfully.

We would like to express our sincerest gratitude to our Supervisor Dr.Satyendra Nath Biswas (Ph.D., P.E), Professor, Department of Electrical and Electronic Engineering, Ahsanullah University of Science and Technology, Dhaka, Bangladesh who has supported and guided us throughout the thesis with patience and immense knowledge whilst providing us the freedom to work in our own manner. His encouragement and useful critiques helped us to complete this research. Without him, it would never have been possible. One simply could not wish for a better or friendlier supervisor.

Words fail to express our gratitude for the love and support that we got from our parents throughout the process of researching and writing the thesis paper.

Table of Contents

List of Figures

List of Symbols and Abbreviations

VLSI - Very Large Scale Integration

SOC - System on Chips

IC - Integrated Circuit

CMOS - Complimentary Metal-Oxide Semiconductor

SRAM - Static Random Access Memory

R - Resistor

C - Capacitor

V- Voltage

I - Current

pMOS - P-type Metal-Oxide Semiconductor

nMOS - N-type Metal-Oxide Semiconductor

WL - Word Line

RWL - Read Word Line

GND - Ground

MSB- Most Significant Bit

LSB - Least Significant Bit

BL - Bit Line

WE - Write Enable

PC - Pre-charge

SAE - Sense Amplifier Enable

RBL - Read Bit Line

WBL - Write Bit Line

Vth -Threshold Voltage

SIA- Semiconductor Industry Association

MOSFET - Metal-Oxide Semiconductor Field-Effect Transistor

PI - Power Integrity

SI - Signal Integrity

DRC - Design Rule Checker

PDP - Power Delay Product

CNTFET- Carbon Nano Tube Field Effect Transistor

FinFET- Fin-Shaped Field Effect Transistor

Abstract

SRAM is intended to replace DRAMs in systems that demand extremely low power consumption by acting as an interface with the CPU. Since SRAM consumes a significant portion of the total power and die area in high-performance CPUs, low-power SRAM design is essential. The conditions for functioning in the submicron/nano ranges must be met by an SRAM cell. SRAM cells are significantly impacted by the scaling of CMOS technology, which results in large electrical leakage current and unpredictable electrical characteristic fluctuations. The SRAM cell has a significant mismatch in transistor threshold voltage due to the random variation of electrical properties. Due to the SRAM cell's tendency to be unstable, low power supply operation is challenging to accomplish. A 9T SRAM cell at 45 nm, 35nm, and 22nm feature size in CMOS is proposed to accomplish low-power memory operation. Initially, this paper presents the design of 9T SRAM cell considering low power consumption. The paper presents the design of SRAM using Cadence tools and LTSpice simulation software.

Chapter 1

Introduction

1.1 Introduction

The advancement of semiconductor industry due to scaling has resulted in tremendous capabilities of today's IC and their pervasive use in almost all modern electronic devices. The advancements of semiconductor technology have boosted the rapid growth of very large scale integrated (VLSI) System in our day-to-day life. In order to meet the growing demand of performance, the amount of embedded or on-chip memory in microprocessor and systems-on-chip (SOC) is increasing, as much as 70% of the chip area is now dedicated to embedded memory, which is primarily realized by the Static Random Access Memory (SRAM).

Microprocessors and systems-on-chip (SOCs) are used in a variety of applications. Such as:

- smart-phones

-Gaming devices

-Computer

-Smart Cars

-Medical Equipment.

SRAM:

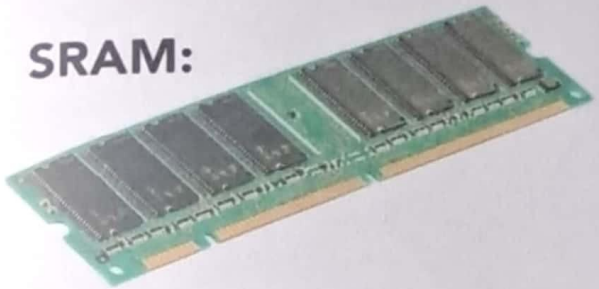


Figure 1.1: SRAM (Static Random Access Memory) [1]

Since the performance demand of users is constantly increasing, it is critical to achieve as high performance as possible at the lowest possible power dissipation. An approach to meet this demand of performance is to increase the memory embedded on the same chip with the microprocessor.

Depending on technology devices performance varies. Like 22nm Technology's device performance is different from 45nm technologies. With modernization for high performance, we are using more complex technology and the design of SRAM for more efficient output.

Semiconductor Industry Association (SIA) have a regulation which states that more than 50% of the area of a typical IC design should be occupied by the embedded memory. And at present 70% of the chip area in present microprocessor is dedicated for memory. [2]

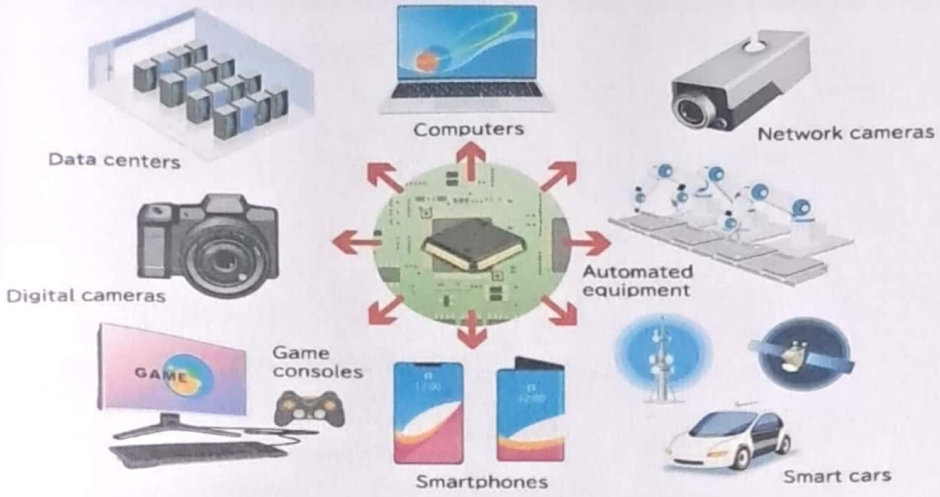


Figure 1.2: Various uses of SRAM

1.2 Background of SRAM design

Memories are designed by means of transistors in conventional method. SRAM or Static Random Access Memory plays an important function in the building of a memory system, and the SRAM occupies almost above 90% of die vicinity in a chip of any system. [3]

In SRAM, all information has been saved in flip-flop. Flip-Flop contains every bit of this RAM. Flip-Flop makes use of 4-6 Transistors for making a memory cellphone and its circuit does not want to refresh continuously. SRAM helps to store each bit with the use of bistable latching circuitry, and generally it used six MOSFET to store each memory bit, but more transistors come to be at smaller nodes.

A MOSFET is a four-terminal device having source(S), gate (G), drain (D) and body (B) terminals. In general, the physique of the MOSFET is in connection with the source terminal therefore forming a three-terminal gadget such as a field-effect transistor. MOSFET is

usually viewed as a transistor and employed in both the analog and digital circuits. This is a simple introduction to MOSFET.

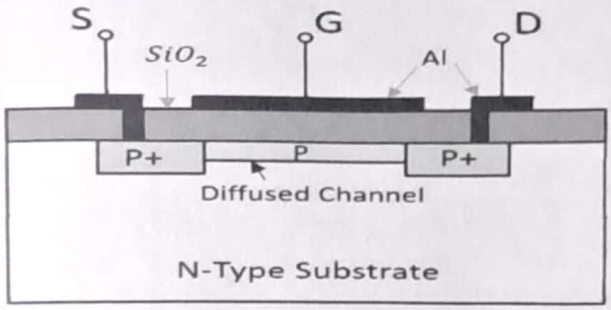


Figure 1.3: Basic Structure of P-channel MOSFET [4]

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor machine that is extensively used for switching purposes and for the amplification of electronic indicators in electronic devices. A MOSFET is either a core or built-in circuit the place it is designed and fabricated in a single chip because the gadget is available in very small sizes.

Here we used two kinds of MOSFET, these are

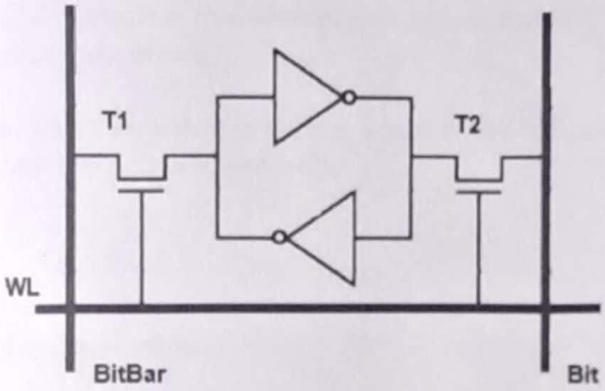
1. P-Type MOSFET

2. N-Type MOSFET

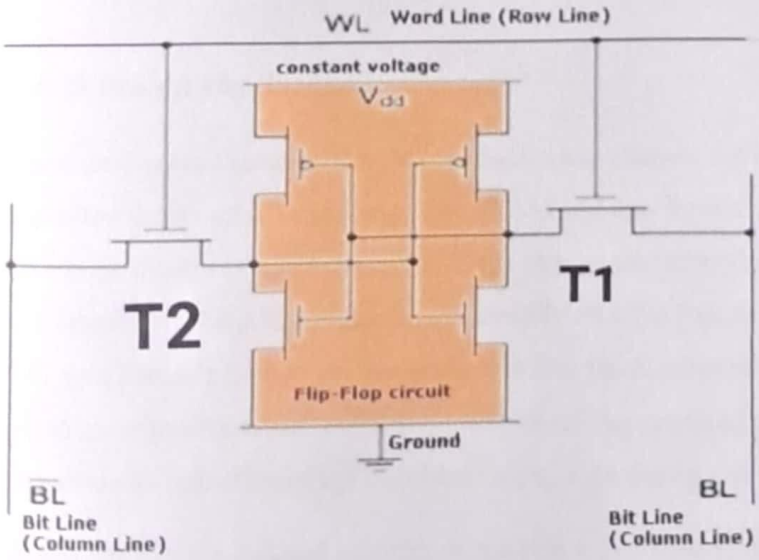
1.3 SRAM Circuit Design and Operation

Static Random Access Memory mobile phone is designed with two inverters, which are cross-linked like latch form. This latch is made connection to two-bit line alongside with two transistors T1 and T2. Now both transistors are capable of altering their modes (open or

close) beneath manipulate of word line, and this entire method is managed with the aid of tackle decoder. When phrase line goes to ground degree then both transistors get grew to become off, and latch starts off evolved to retain very own state.



(a)



(b)

Figure 1.4: Basic circuits of SRAM (a)&(b)

1.3.1 Read operation

Both switches T1 and T2 are closed whilst activating the word line. When, cell comes to state 1 then the signal flows in high amount on the b line and the other signal flows in low quantity on b' line. The opposite is true when mobile goes to nation 0. Finally, each b and b' get complement of each other's.

Sense/write, which are linked in the rear aspect of two bit lines, they monitor their states and finally convert into output respectively.

1.3.2 Write Operation

In the write operation, Sense/Write circuit allows to pressure bit strains b, and it complement b', and then it gives accurate values on bit line b and b' as nicely as go to set off word line. [6]

1.4 SRAM design challenges

Static Random-Access Memory (SRAM) has been a key element for logic circuitry since the early age of the semiconductor industry. The SRAM cell usually consists of six transistors connected to each other in order to perform logic storage and other functions. [7]The size of the 6T (6 Transistors) SRAM cell has shrunk steadily over the past decades, thanks to Moore's Law (Moore's Law refers to a prediction that the number of transistors that can be packed into a computer processor of a given size should be expected to be double every two years) and the size reduction of the transistors along with denser wiring & contacts.[8]

In particular, the process induced variation in transistor threshold voltage and dimensions, the higher leakage power consumption, and increased sensitivity to external noise sources, such as radiation induced single event voltage transients have become key concerns to address. [9]

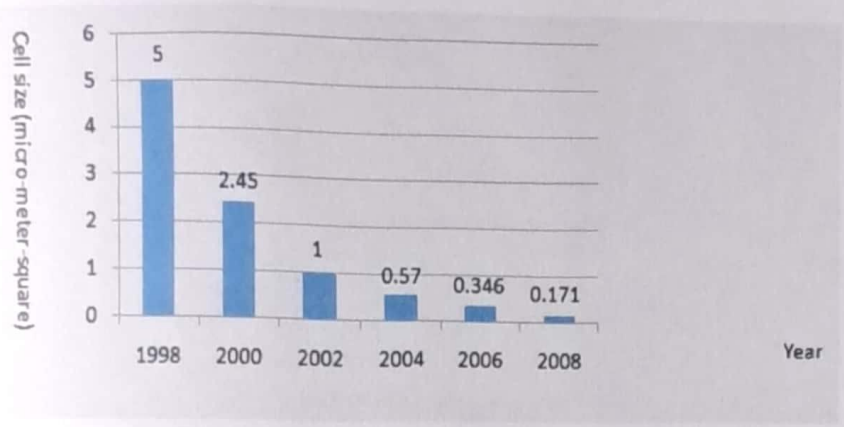


Figure 1.5: Scaling Trend of SRAM bit-cell in size [9]

Like A-16 bionic chip consist of 16 billion transistors which are a complicated circuit. Though its size is small, it consists of billions of transistors. So, designing it is a massive challenge.

1.4.1 Leakage power consumption

The energy consumed in a gadget is composed of two kinds and one of them is leakage power. Smaller than 90nm technological know-how, leakage power has turned out to be the dominant consumer of energy. Power reduction strategies can be used to reduce the consumption of power. [10]

Leakage energy is a characteristic of the supply voltage Vdd, the switching threshold voltage Vth, and the transistor size.

PLeakage = f (Vdd, Vth, W/L)

Where Vdd = the furnish voltage, Vth = the threshold voltage, W = the transistor width and L = the transistor length.

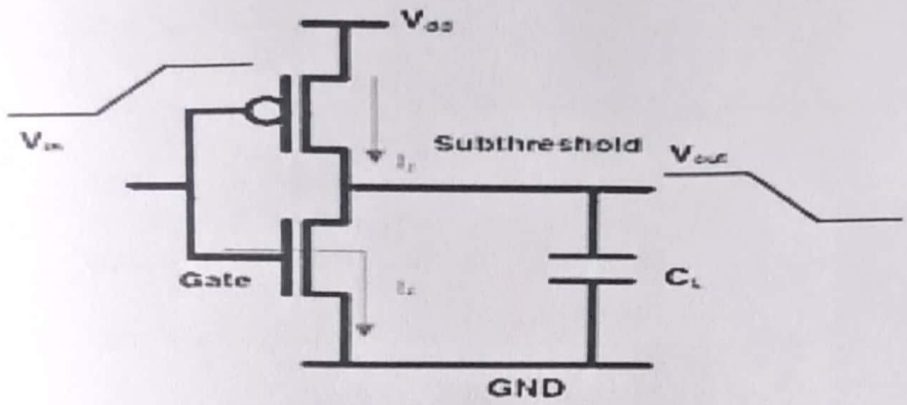


Figure 1.6: A CMOS inverter

SRAM leakage strength consumption plays the cardinal role in sustaining battery lifestyles of portable devices. The lower the leakage contemporary, the higher the would-be battery life [11]. The portable or cellular units additionally have the threat of becoming very hot and doubtlessly explode in intense cases and such a situation would be threatening for the user. Added to this we can say that the higher leakage strength would force the designers to use a higher battery pack. However, a larger battery pack would make the cellular system heavier and as an end result the mobility would be misplaced to a certain extent.

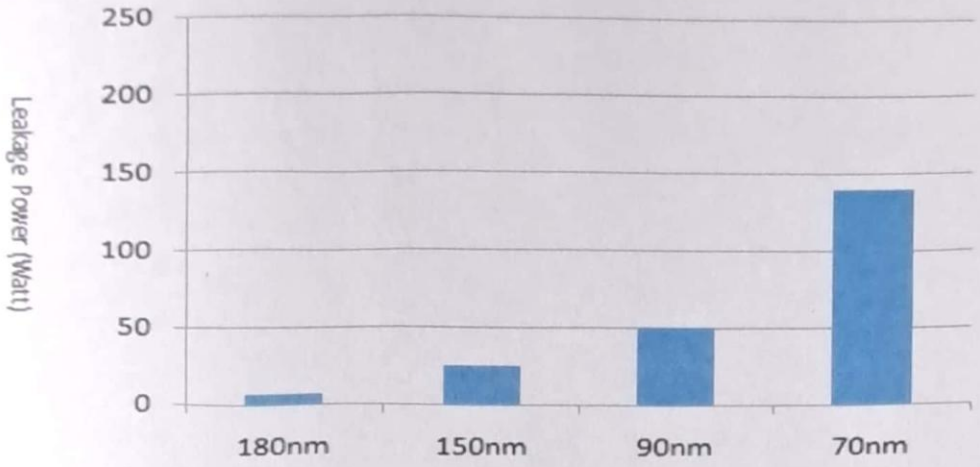


Fig 1.7: Leakage Power consumption in nm technology [11]

1.4.2 Cell area

One of the most important factors for SRAM cell design is the cell area. The cell area determines about two-thirds of the total chip area. Increasing the density of SRAM caches provides an effective method to enhance system performance. [12]

In 18nm technology, the cell area of conventional 6T SRAM is 1.079 um^2, 7T SRAM cell area is 1.25 um^2 and 8T SRAM cell area is 1.28 um^2.

From the cell area comparison, we can see conventional 6T requires less area than 7T and 8T.

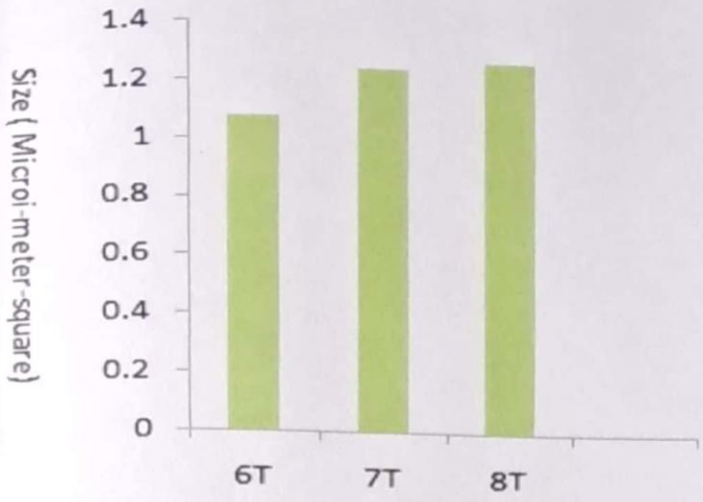


Fig 1.8: SRAM Cell area Comparison

1.5 Objectives

The main challenges that the researchers have always been facing are in maintaining all the components up to the mark for making better electric device power consumption and propagation delay.

In this dissertation we have tried to rectify the drawbacks that the conventional models have by adding three more transistors. Mainly, this thesis focuses on the improvement of:

1. Less power consumption

2.Better propagation delay

3. Fast operational speed

Chapter 2

Literature Review

2.1 SRAM Architecture

A typical SRAM consists of an array of memory cells along with some peripheral circuits. The peripheral circuits include the row decoder, column decoder, address buffer for row and column decoders, sense amplifier, precharge circuitry, and data buffers. While the construction of the SRAM array can be very complex depending on the memory size, area, and speed requirements, a basic array consists of 2L rows and Nx2K columns of cells. Here L is the number of address bits for the row decoder K is the number of address bits for the column decoder, and N is the number of bits in a word. There are 2L word lines, only one of which is activated by the row decoder based on the row address bits (bits A0 to AL-1 in Figure 2.1) at a given instant [13].

On the other hand, K address bits are decoded to select one of the N-bit words from a given row. Most of the recent microprocessors operate with 64-bit words and hence are referred to as 64-bit processors. Thus, the SRAM array for such systems will have 2K x 64(or 2K+6) columns of cells in total. Usually, K and L are selected in such a way that the overall array assumes a square shape when laid out. Thus, 2K+6 = 2L or K+6=L can be tentatively used for a layout-optimized array for square-shaped cells. The choice of using row-select bits as MSB and column-select bits as LSB of the entire address bits or vice versa is arbitrary. The timing of the activation of the sense amplifier, write driver, decoders and other peripherals are controlled by a timing circuitry. The read/write (R/W) signal determines whether the SRAM is to be read or written.

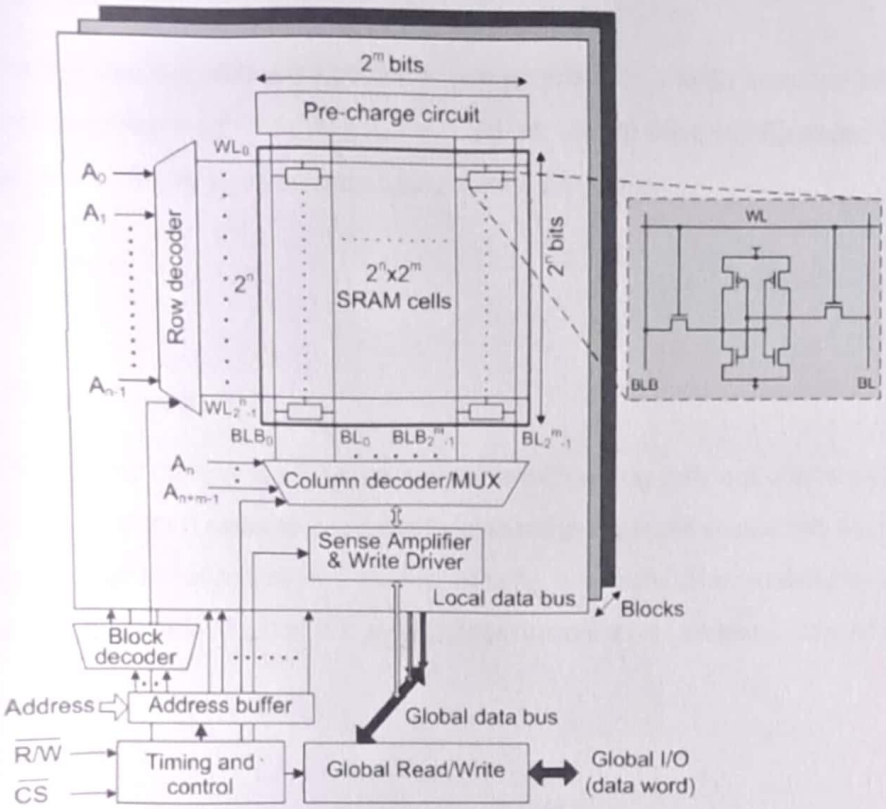


Figure 2.1: A typical SRAM architecture. [13]

SRAM consists of the following circuits:

- **SRAM cell:**

A cell that stores the binary data bit is the main part of the SRAM design. It is made up of access transistors and a latch. The access transistors enable read and write access to the cell and provide isolation, while the latch saves the data bit.

• **Row Decoder:**

The row decoder activates a particular row by selecting it in the array and asserting the corresponding word line (WL) signal. They are used to drive wordlines and it has active high output in SRAM. It asserts only a single output at a time.

•**Column Decoder:**

The column decoder is a 2(M) multiplexer which selects only one output using the M select lines. It makes it easier to insert multiple words in a row and selects one word when reading or writing. The aspect ratio of the SRAM array is brought closer to unity by using many words in a row so that the WL and BL capacitances are of the same order of magnitude.

• Sense **amplifier:**

In a read operation, a sense amplifier is used at every column to read the selected word through the bit lines. The stored data inside the SRAM cell appears on BL and the complement of the stored data appears on BLBar. However, the data is not directly read from the bit lines. If the data is directly read from the bit lines, then one of the bit lines must be discharged to 0V. Since the bit lines are highly capacitive, discharging a bit line to 0V would make the subsequent pre-charging consume a significant amount of power. In addition, SRAM cells are made as small as possible to maximize the memory capacity in each silicone area. The current driving capability of the SRAM cell's read discharge path is very low. If such a low current drive is used to discharge the highly capacitive bit lines, it would take a large amount of time. Sense amplifier is used to avoid these problems.

• **Write Driver:**

The write driver enables writing into an SRAM cell by pulling down one of the bit lines of the selected column from the precharge level to below the write margin. [13] Typically, the Write Enable (WE) signal activates the write driver. The order in which the word line and WE are enabled is not crucial for the correct write operation.

For each column, only one write driver is required. Additionally, each column just needs one write driver. As a result, the layout is not complicated by the vast space needed by the pull-down transistors of a write driver.

• **Timing and Control Circuits:**

Timing circuits are used to synchronize bits whereas control circuits are used to share status data, instructions, and results. The timing and control circuits generate the precharge (PC), word line (WL), sense amplifier enable (SAE), and write enable (WE) signals to ensure correct read and write operations. [13]

2.2 Conventional 6T SRAM Cell

The 6T SRAM cell has been used by the semiconductor industry in today's SRAM-based memory designs, VLSI designs, and microprocessors. The most widely used SRAM bit-cell is the six-transistor (6t) cell shown in the figure:
The architecture consists of a back-to-back CMOS inverter latch and two access transistors. The latch holds the data bit while the access transistors are used for read and write operations. Access transistors also isolate the cells from the bit lines (BL and BLBar) when they are not accessed. As opposed to DRAM, an SRAM has to provide non-destructive read operation and the ability to indefinitely retain data without any refresh operation (given the power is supplied to the cell).
A conventional 6T SRAM of two cross-coupled inverters is shown in the figure: The SRAM consists of two pMOS (M3 & M2) and 4 nMOS (M1, M4, M5&M6) transistors, where M5 and M6 transistors are also known as the access transistors.

The storage nodes are Q and Qbar. These cross-coupled inverters forming the latch act as a storing element, i.e., each bit is stored in the latch and access transistors are enabled/disabled using word line (WL). When the word line is low, access transistors are disabled. At this time, read or write operations cannot be performed, and hold state is required. At this state, latch can hold bit as long as the voltages remain at Vdd and GND. When the word line becomes high, access transistors M5 and M6 are enabled, and at this stage read and write operations can be performed. [14]

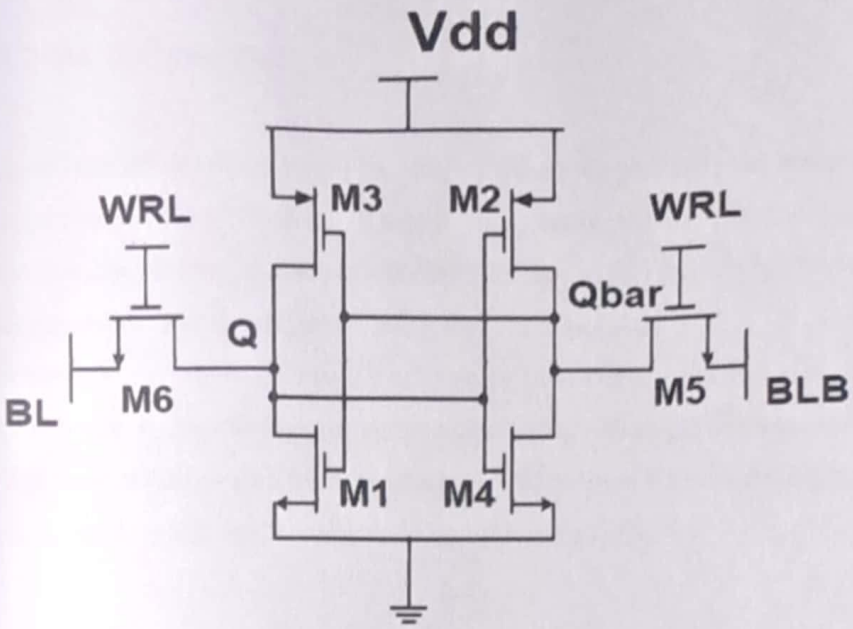


Figure 2.2: A conventional 6T SRAM structure

2.2.1 Write Operation

In write mode, The bit line acts as input while performing the write operation. The value to be written into the memory cell is provided with the help of bit lines replacing its originally stored bit.

To perform write operation, the access transistors (M5&M6) are enabled using word line (WL=1). The required data to be written is given to bit line (BL), and its complement is applied on bit line bar (BLBar).

That means if we want to write "1" to the SRAM cell, we must provide "1" to bit line (BL) and "0" to bit line bar (BLBar). As a result, M3 and M4 transistors are turned on. On the other hand, M1 and M2 transistors are turned off.

When the state of latch is changed the word line is deactivated (WL= "0"), and thus the required data is stored to "Q" written to the cell. In read mode, SRAM cell can communicate its stored data.

2.2.2 Read Operation

The bit lines act as output during the read operation. To perform read operation, the word line is kept at high (WL= "1") which activates the access transistors (M5 &M6). During the read operation, the bit line (BL) and bit-line bar (BLBar) should be completely detached from the memory cell so that it does not interfere with the stored data.

We were able to achieve this isolation by using two extra transistors which were not supplied with any gate voltage during the read operation. Both the output lines are applied to the input of the sense amplifier which finally gives the information of the stored bit by amplifying the data. Sense amplifier helps in determining the value of 'Q'.

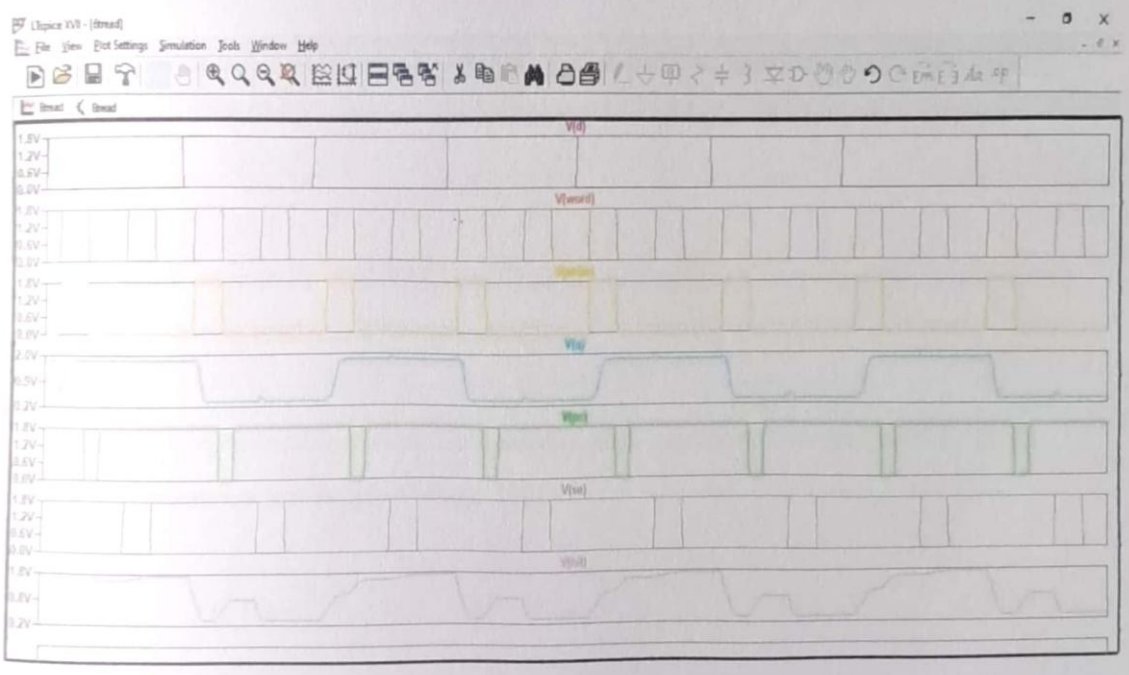


Figure 2.3: Read / Write operation of conventional 6T SRAM

2.3 Limitations in 6T SRAM cell

When using the standard 6T (six transistors) SRAM cell configuration, significant issues have been found.

- The power dissipated during read and write operation helps to determine the battery life of portable devices. Due to the high-power consumption of the traditional 6T SRAM, battery life is reduced.

- The speed of SRAM is determined by the delay. The standard 6T cell exhibits a significant time delay and leads to slower operation.

- Leakage power is a high priority for designing high-performance processors. The leakage power of the 6T SRAM is a major source of power loss and the reason for the cell's low efficiency.

- Although this commonly used SRAM cell has the advantage of very less area, it cell shows poor stability during read and write operation.

- The cell is most vulnerable to noise compared to hold operation. The read stability of the 6T cell deteriorates at low supply voltage. [15]

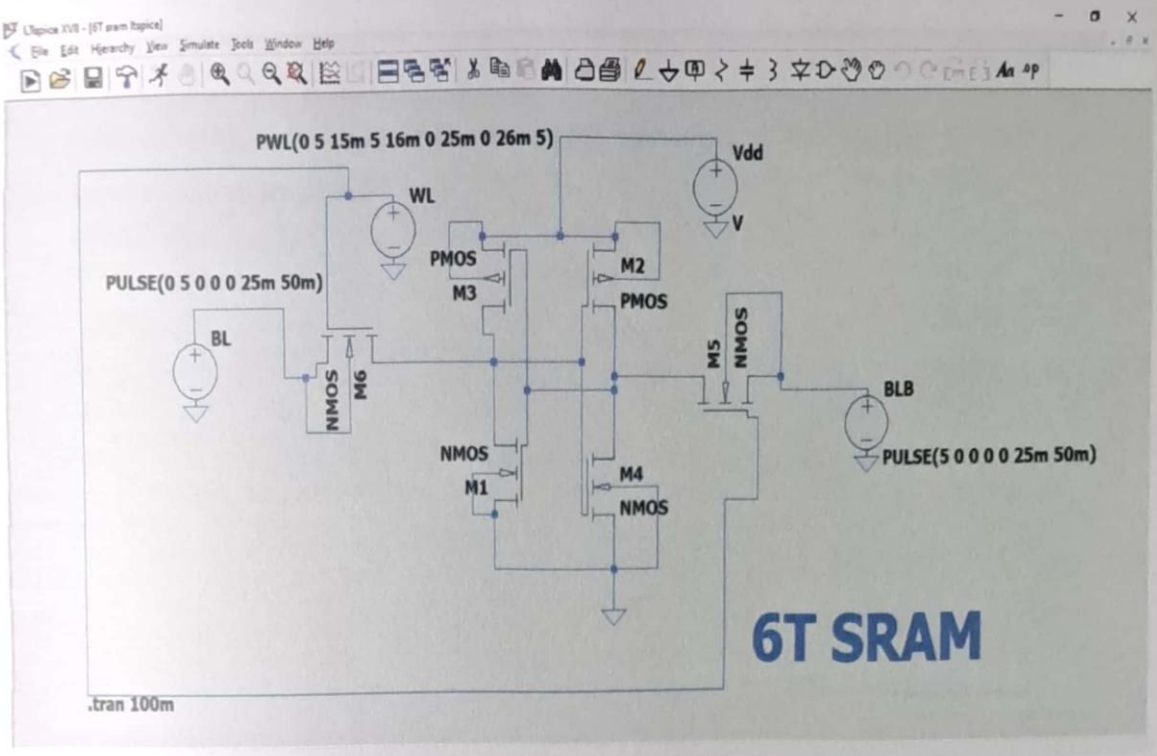


Figure 2.4: LTSpice simulation of conventional 6T SRAM cell

Therefore, to achieve low-power operation various literature can be found on designing SRAM cells. The common method to meet the objective of low-power design is to add more transistors to the original 6T cell.

Several cell architectures have been suggested to meet these requirements.

In this article, some of the cell layouts have been simulated, analyzed and results of their performances have been compared.

2.4 7T SRAM Cell

The cell has been designed using 7 transistors and 45nm technology to reduce power consumption. In this cell, the read operation runs from the left side and the write operation runs from the right side. Data saved in Q and QB nodes is held in transistors M5, M6, and M7.M1 and M2 transistors are added to the proposed 7T cell to improve cell stability during read mode.

The stability of reading mode is increased because the M2 transistor isolates the Q node from the reading access transistor. In order to reduce leakage current, the M6 transistor is employed as a high voltage threshold. [16]

The proposed cell has ideal features like low power consumption, high stability, low delay, high speed than conventional 6T.

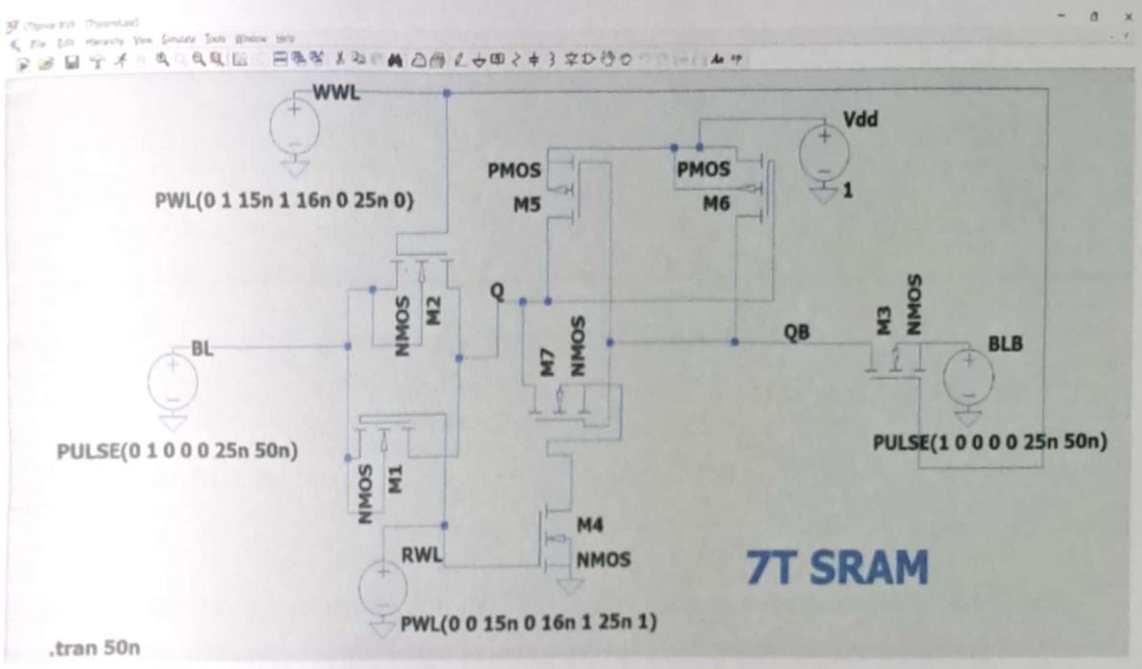


Figure 2.5: LTSpice simulation of conventional 7T SRAM cell

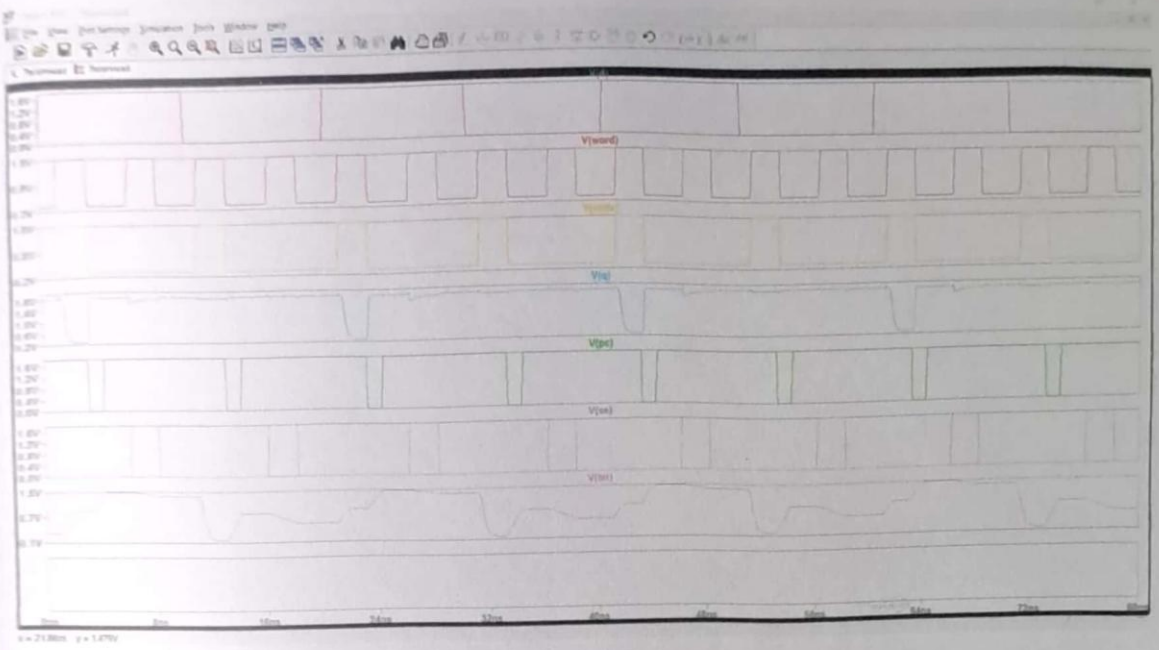


Figure 2.6: Read / Write operation of conventional 7T SRAM

2.5 8T SRAM Cell

The transistor configuration (M1 through M6) is identical to a conventional 6T SRAM cell. Two more transistors are added to the existing structure of 6T SRAM cell. These extra transistors M7 and M8 are used to reduce leakage current. The write operation of 8T SRAM cell is same as to the conventional 6T SRAM. This cell overcomes the problem of data storage destruction during the read operation, eliminates stability issue encountered in a 6T SRAM cell and high read stability is attained [17]. Leakage current through M7 may result in a severe voltage and significant power loss.

Though the transistor count increased the power consumption, the drawbacks in 6T SRAM are lowered in 8T SRAM.

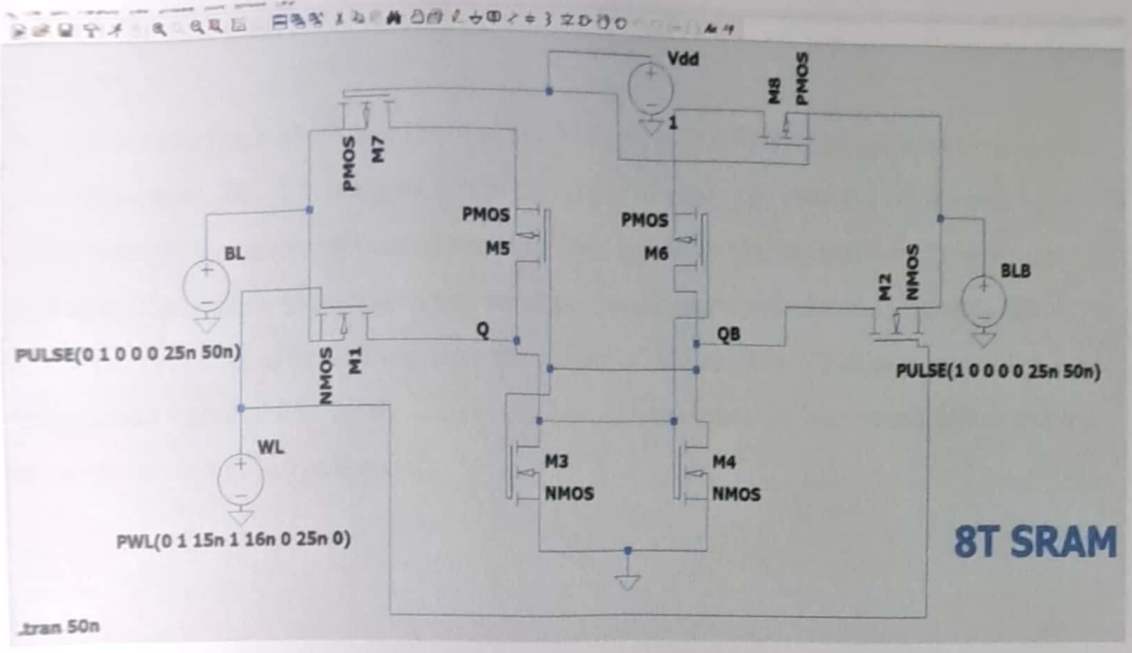


Figure 2.7: LTSpice simulation of conventional 8T SRAM cell

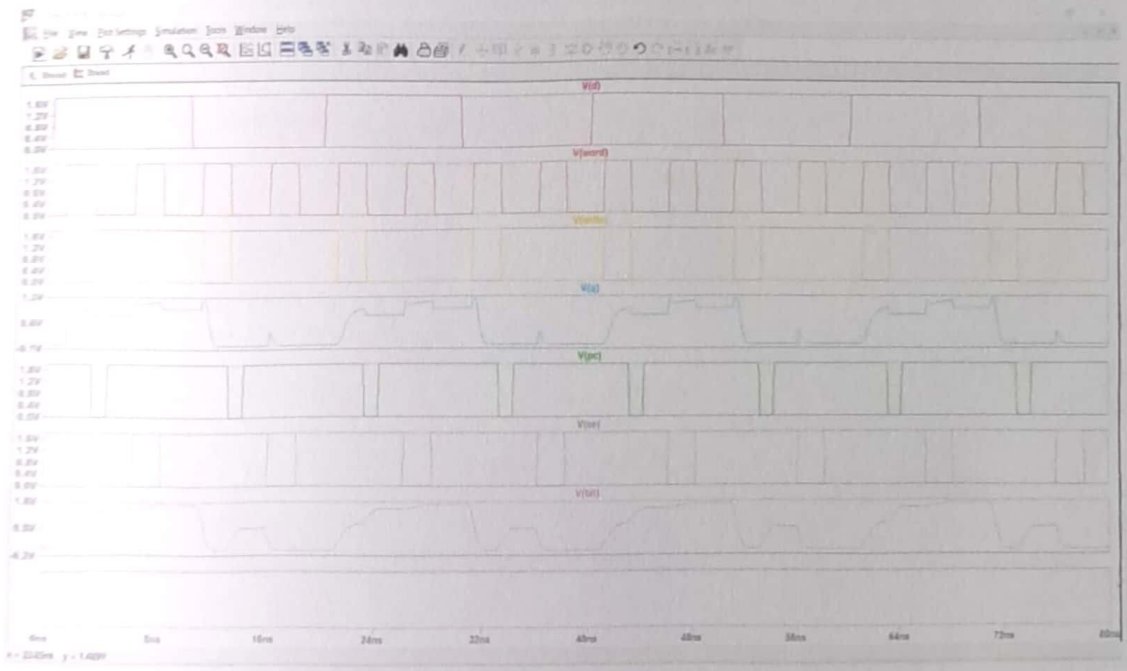


Figure 2.8: Read / Write operation of conventional 8T SRAM

2.6 9T SRAM Cell

The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell with minimum-sized transistors. The data is stored within this upper memory sub-circuit. [18] A write signal (WR) controls the two write access transistors (M2 and M4). The bit-line access transistors (M1 and M3) and the read access transistor make up the lower sub-circuit of the new cell (M9). The data kept in the cell regulates the actions of M1 and M3. M9 is controlled by a distinct read signal (RD). The 9T SRAM cell has high read stability but the cell data is prone to corruption due to external noise.

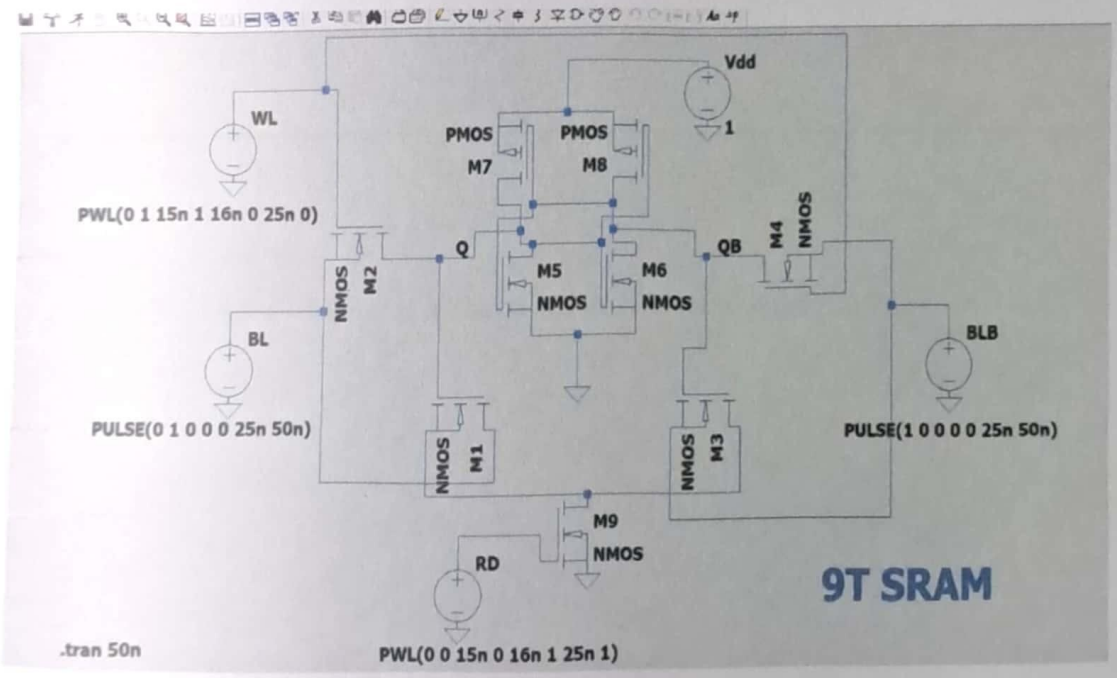


Figure 2.9: LTSpice simulation of conventional 9T SRAM cell

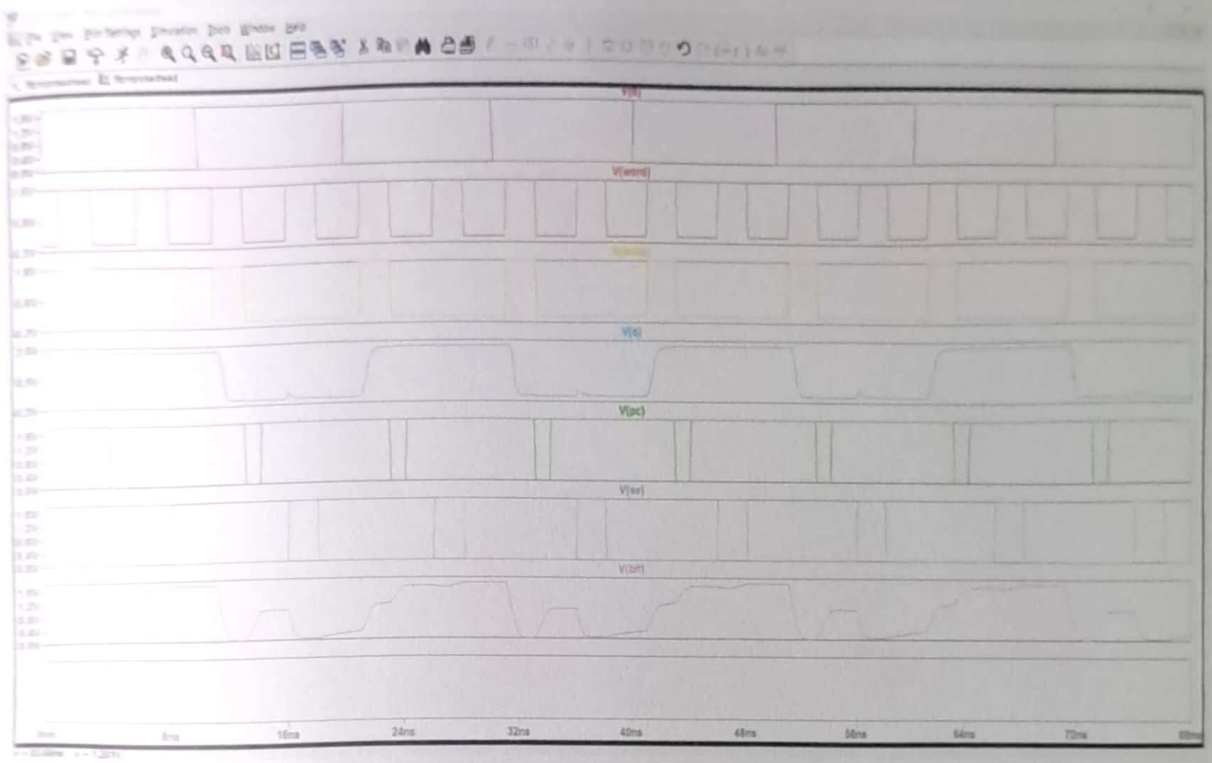


Figure 2.10: Read / Write operation of conventional 9T SRAM

Chapter 3

Proposed 9T SRAM cell

3.1 Designing Proposed SRAM cell

We have proposed a 9T SRAM to significantly reduce the several limitations of the conventional 6T SRAM cell. This cell will provide lower energy consumption and longer battery lifespan for portable devices with demanding speed requirements.

The read, hold operation, efficiency, and overall performance will all be enhanced by the additional three transistors added to the 6Ttopology.The design and simulation results were carried out using LTSpice and Cadence Virtuoso to evaluate the performance of proposed 9T SRAM cells.

3.2 Proposed Low Power 9T SRAM cell design

In the designing of the proposed cell, three more transistors are added to the basic 6T SRAM cell. The M7, M8, and M9 transistors have been added to the SRAM architecture to reduce power consumption drastically, reduce leakage current and facilitate faster operation. The transistor configuration (M1 through M6) is identical to a conventional 6T SRAM cell. The results were obtained for 45nm,32nm, and 22nm CMOS technologies using the LTspice simulator [20].

By disabling the access transistors when reading, the read de-couple circuit isolates the basic memory component and reduces noise. Both single-ended read and double-ended write operations are included in this cell. Write operation is controlled by the WR signal, whereas read operation is controlled by the control signals RD and RDBar. Transistors M8 and M9 form a transmission gate connected to RBL.

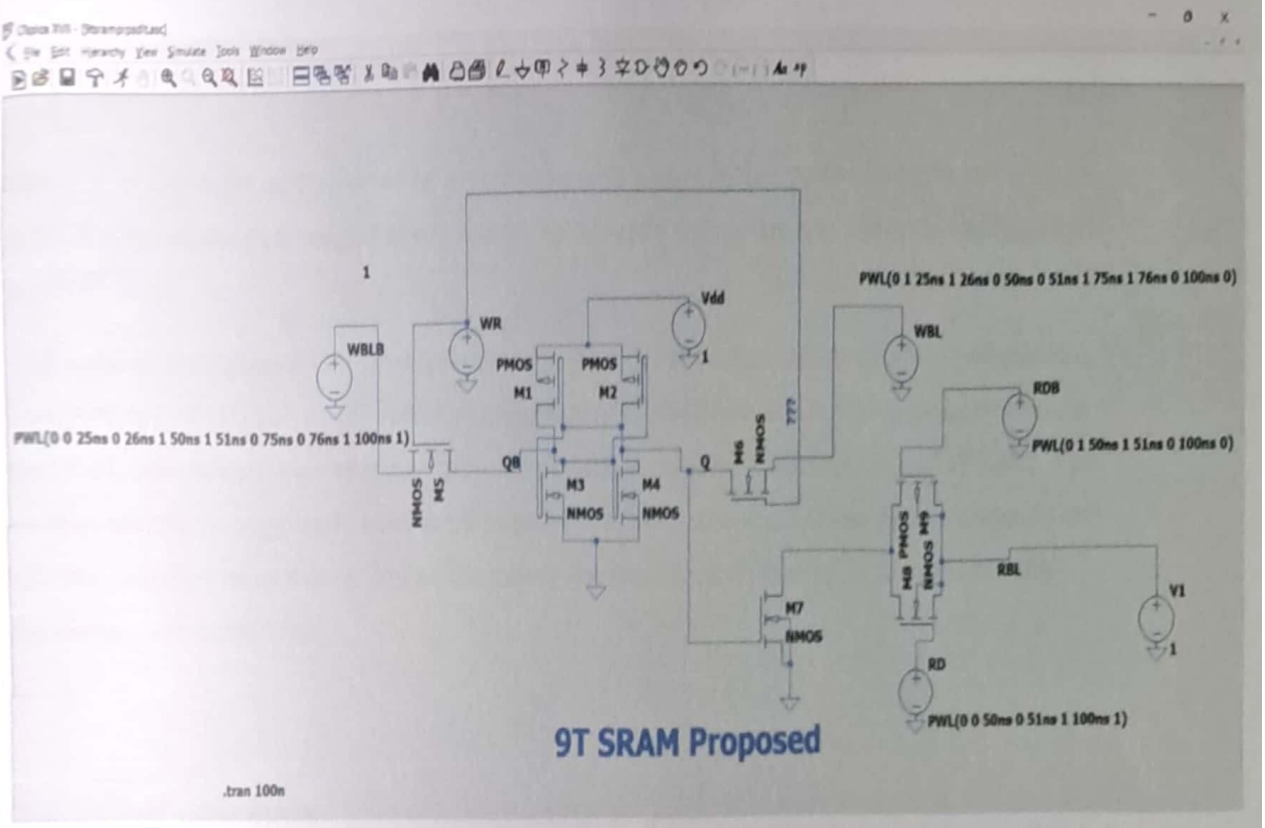


Figure 3.1: LTSpice simulation of the proposed 9T SRAM cell

3.2.1 Read operation

The aim of the read operation is to successfully recover the data stored on the inverter pair without causing distortion in any way. Assuming logic "1" is stored at node Q. The read bit line (RBL) is precharged to a value as close to VDD as possible.

The read operation is initiated by asserting the control signal RD, enabling pass transistor M7 and transmission gate (M8, M9). A read operation can be performed by discharging the RBL through M8-M9-M7. The values are stored at Q and it is coupled to the gate terminal of transistor M7.

3.2.2 Write operation

The aim of the write operation is to inverse the data that is stored on the inverter pair. While WBLB stays at the precharged level, the write circuitry forces the write bit line (WBL) to the logic"0" level.

The write control signal WR is asserted, turning on the access transistors, while keeping the node voltage of QB below the threshold voltage of the M3 transistor. The writing occurs on the WBL side where the voltage at node Q starts to drop from the initial logic "1" level. The second inverter is triggered because of positive feedback; the logic levels on the nodes Q and QB are switched once this voltage falls below the threshold voltage of M1. Thus, writing operations are carried out.

3.2.3 Hold operation

As the access transistors are in the off state and neither the write control signal (WR) nor the read control signal (RD) is active, there is no conduction taking place to discharge the Q and QB node, and the data stays unchanged.

3.3 Advantages

1. The proposed design reduces the average power consumption significantly.

2. Endures less leakage power.

3. Less read time delay due to read-decoupled circuit.

4. Enhances stability.

Chapter 4

Comparison of proposed 9T SRAM Cell with other topologies

The simulation framework utilized for the thesis is described in this section. Proposed SRAM cells have been compared with the conventional SRAM cells at different technologies in terms of power dissipation, delay, power delay product, leakage current, and area.

4.1 Software for Simulation

Considerable simulations are carried out using LTspice [19] with the help of the PTM transistor model [20] (45nm,32nm,22nm). The simulation results of write operation, read operation, hold operation performance, and comparison with the conventional 6T and 10T SRAM cell in terms of time delay, and power dissipation. The Cadence design system software tool [21] was used to draw the layout of the proposed and conventional cells.

4.1.1 LTspice Simulation Software

LTspice is a high-performance SPICE simulator, schematic capture, and waveform viewer with enhancements and models for easing the simulation of switching regulators. Our enhancements to SPICE have made simulating switching regulators extremely fast compared to normal SPICE simulators, allowing users to view waveforms for switching regulators in just a few minutes.

We have used the LTspice IV, Macro Models for 80% of Linear Technology's switching regulators, over 200 op amp models, as well as resistors, transistors, and MOSFET models. [19]

4.1.2 Cadence Design System

The complexity and performance requirements of today's semiconductor packages continue to increase with design resources remaining static for most organizations- placing a premium on efficiency and productivity. Cadence IC packaging and multi-fabric, co-design deliver automation and accuracy to expedite the design process as part of a comprehensive environment that also includes analysis.

With complex advanced packages, we face power integrity (PI) and signal integrity (SI) issues driven by increasing IC speeds and data transmission rates combined with a decrease in power-supply voltages and denser, smaller geometries. Stacked die and packages, higher pin counts, and greater electrical performance constraints are making the physical design of semiconductor packages more complex. To address these issues, you need advanced PI and power-aware SI Sigrity tools that can be used throughout the design process [21].

4.2 Result and Data Table of various SRAM Structures

Data Table

Parameters	Conventional 6T SRAM	7T SRAM	8T SRAM	9T SRAM			9T SRAM (Proposed)		
				45nm	32nm	22nm	45nm	32nm	22nm
Average Power(nW)	1200	603.54	1050	135.28	93.1	66.14	51.79	35.95	25.33
Propagation Delay(ns)	0.445	0.328	0.786	0.9	0.65	0.545	0.64	0.605	0.505
Vdd	1	1	1	1	1	1	1	1	1
Leakage current(pA)	9.71	7.32	8.41	6.78	7.03	7.34	5.25	6.01	6.55
Area (Normalized)	1	1.37	1.4	2.14			2.2		
Power Delay Product (J)	5.34E-16	1.97E-16	8.253E-16	1.21E-16	6.05E-17	3.6E-17	3.31E-17	2.17E-17	1.27E-17

4.3 Comparison of Power Consumption

A long battery that performs satisfactorily is the primary need for portable gadgets. Power dissipation is the biggest barrier to having a decent battery.

The average power consumption is significantly lower with the proposed SRAM cell. From the graph (Figure 4.1) it is evident that it has the lowest average power consumption when designed with 22nm technology as compared to the 45nm technology. Average power consumption decreases as the technology node scales down [22].
The percentage decrease in total power dissipation from 45nm to 22nm technology node is 51.09%. The 45nm of the proposed cell has 97% less power consumption as compared to the conventional 6T, 95% less than 7T, and 81% less than 9T SRAM cell.

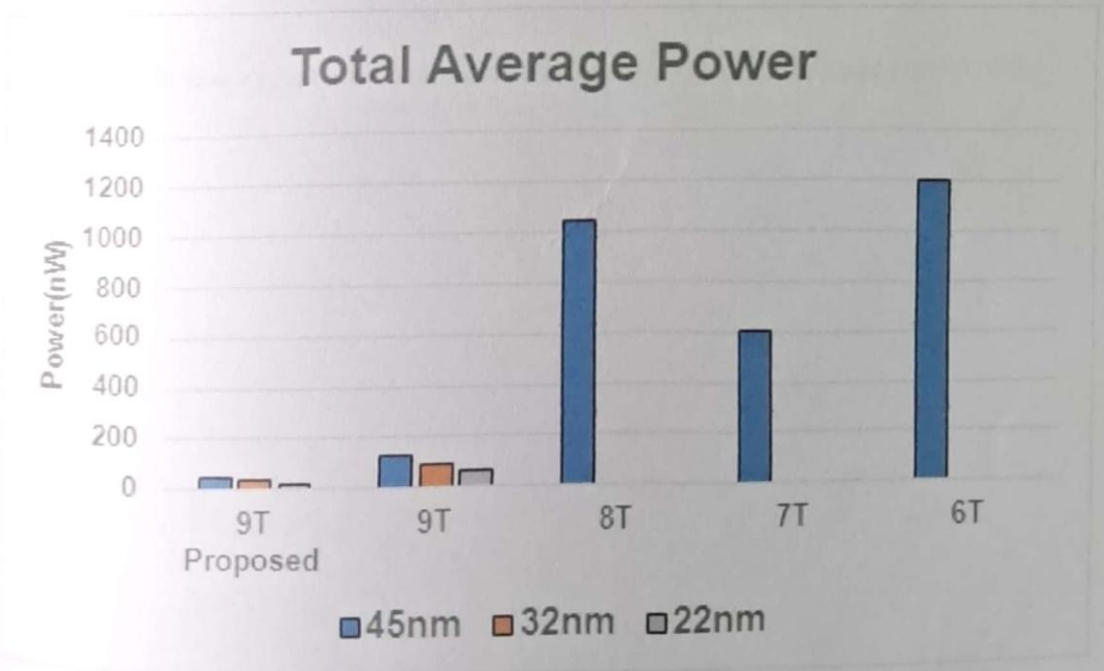


Figure 4.1: Comparison of Average Power Consumption

4.4 Comparison of Leakage current

A crucial factor that every designer must consider during the development of memory cells is leakage current. Leakage current is basically the part of the current that is wasted by being drawn out of the cell through transistors.

The proposed cell was simulated and tested for leakage current using LTspice. By comparing the results, it is clear that the extra transistors M7, M8, and M9 considerably reduced leakage current.

Leakage current is improved with increasing technology nodes. 45nm technology proposed SRAM showed the least amount of leakage current and conventional 6T has the worst amount of leakage current. The leakage current in the proposed structure is reduced by 45% to the conventional 6T, 28% to 7T, 35% to 8T, and 22% to 9T cells.

Figure 4.2 provides a graphical illustration of the comparison of the leakage current of the different cells.

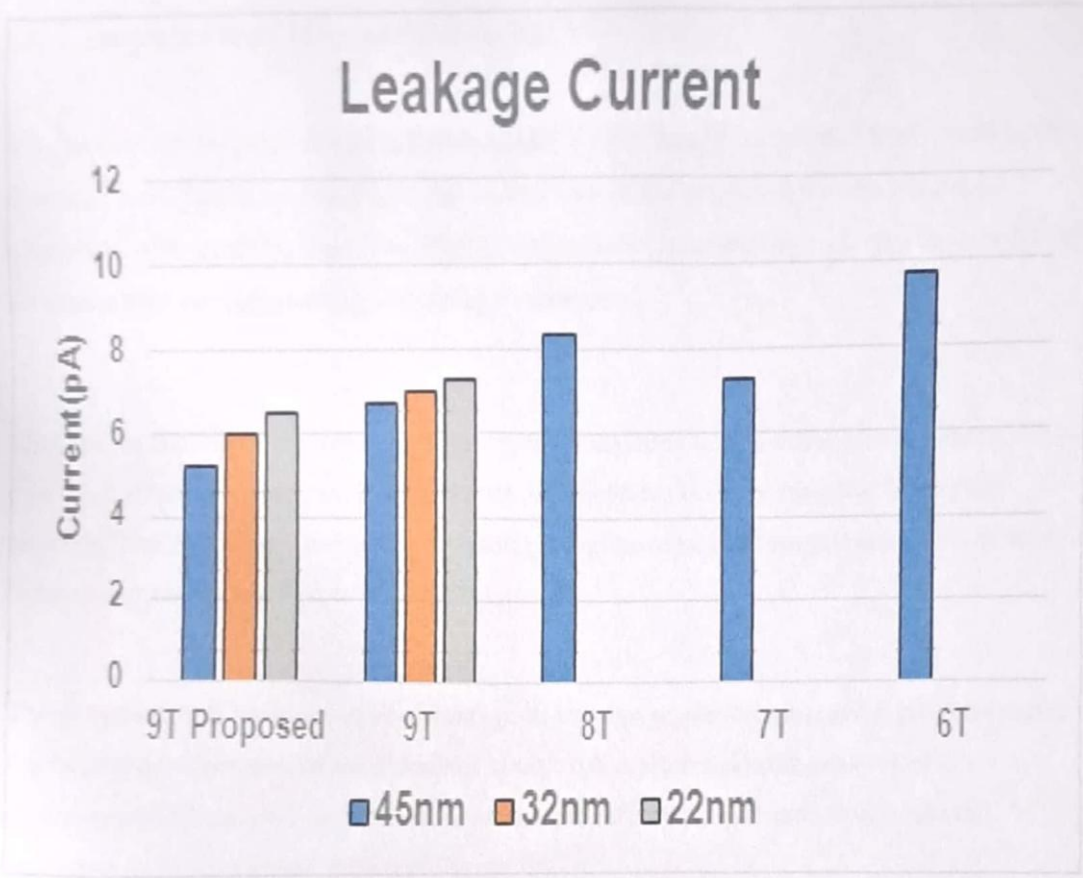


Figure 4.2: Leakage Current comparison of different cells

4.5 Comparison of Normalized Area

The layouts of the proposed 9T SRAM cell,6T,7T,8T, and 9T cells have been drawn in the Cadence tool. The areas have been calculated area of the proposed 9T cell has been compared with other layouts. The DRC (Design Rule Checking) was always kept on in order to ensure that enough spacing was always maintained.

DRC helps the designer avoid placing any two transistors or any other components closely as any such mistake would result in the entire cell malfunctioning during the fabrication process. The areas were calculated by multiplying the measured length and width of each layout using the scale in the Cadence tool.

The proposed cell has a massive advantage in average power consumption, but it occupies the largest area because of the transistor count. It has almost double the area of the conventional 6T cell. 6T and 7T are the most area efficient. The compared areas are exhibited in the bar graph shown in Figure 4.3.

Figure 4.3: Comparison of the normalized area of the proposed 9T cell with other cell structures

4.6 Comparison of Propagation Delay

The difference between the time at which input is applied and the time at which response is obtained is referred to as delay. The transistors that are available are not ideal and the designs are also not perfect, so some amount of delay is present in almost every cell model. The core purpose of designing any system is to reduce the delay which enhances the system's speed.

The proposed SRAM doesn't have the lowest time delay due to flaws in the model. But the cell has a significantly lower time delay as compared to the 8T and 9T topologies and it's closer to the time delay of conventional 6T. It has a 35.75% lower time delay than 8T, 11% and 35.04% higher delay than 6T&8T.

The comparison of the results is done at 45nm, 32nm, and 22nm technology nodes, which shows that the time delay is improved as the channel length is reduced. The propagation delay improved by 21.03% from 45nm to 22nm technology.

The following Figure 4.4 shows the results obtained from the simulation of three technologies and compares them with other cells in a bar diagram.

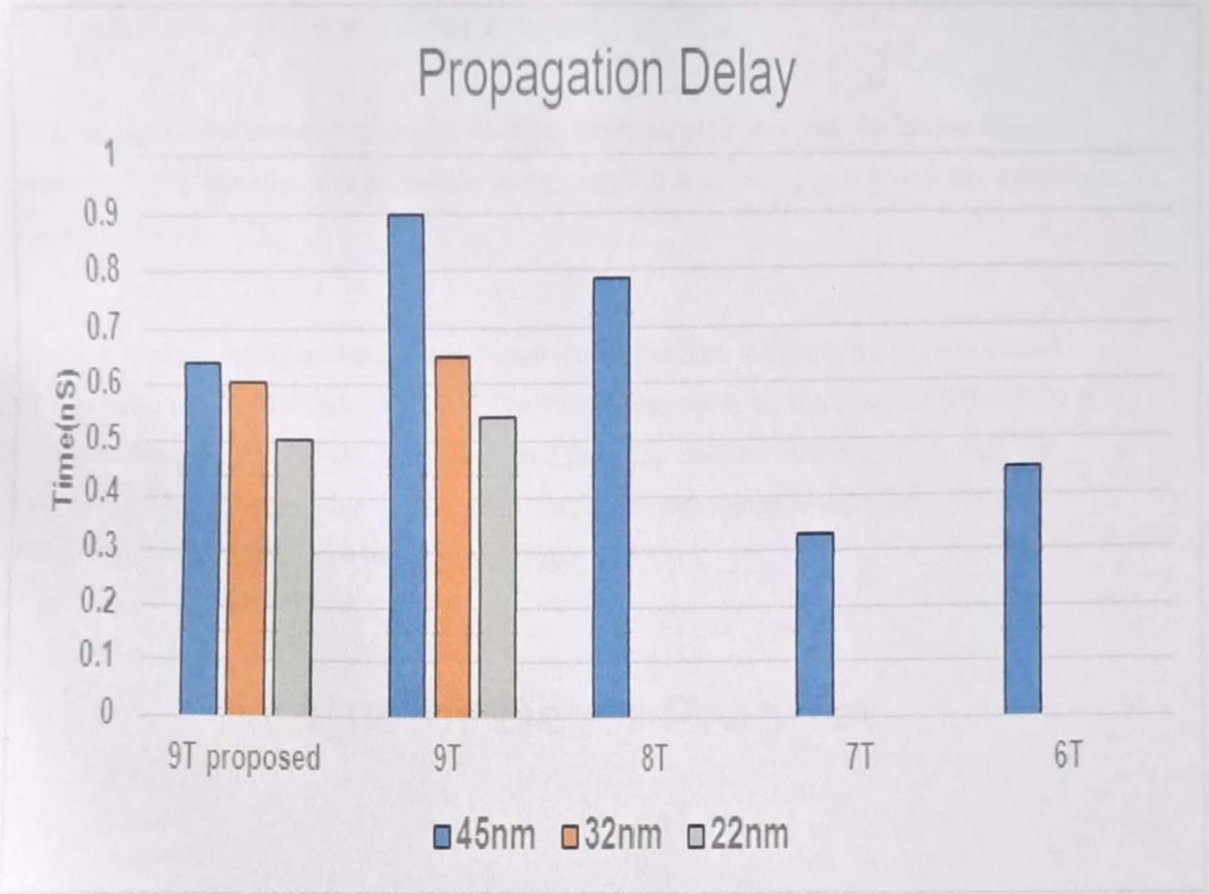


Figure 4.4: Time delay comparison between the proposed model and conventional models

4.7 Comparison of Power delay Product

The average power consumption and the delay are multiplied to create the power delay product (PDP). Because it measures the energy used in a switching event, it is also known as switching energy. [22]

The performance is determined by the Power Delay Product. An energy-efficient circuit design has a low Power Delay Product. The 9T proposed cell has the lowest PDP and the 8T structure has the highest PDP. It is interpreted from fig: that the PDP decreases with the decreasing CMOS technology nodes. Thus, the 22nm technology is the most efficient according to the PDP shown in the graph (Figure 4.5)

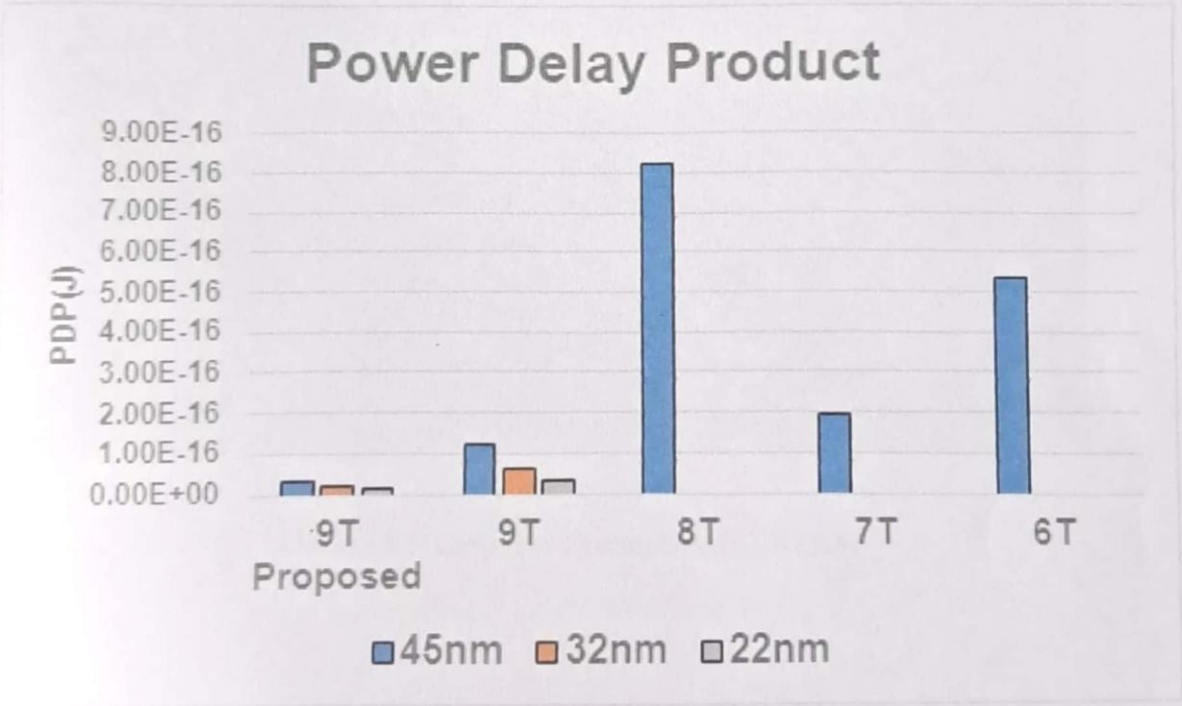


Figure 4.5: Comparison of Power Delay Product

4.8 Layouts of Different Cell Topologies

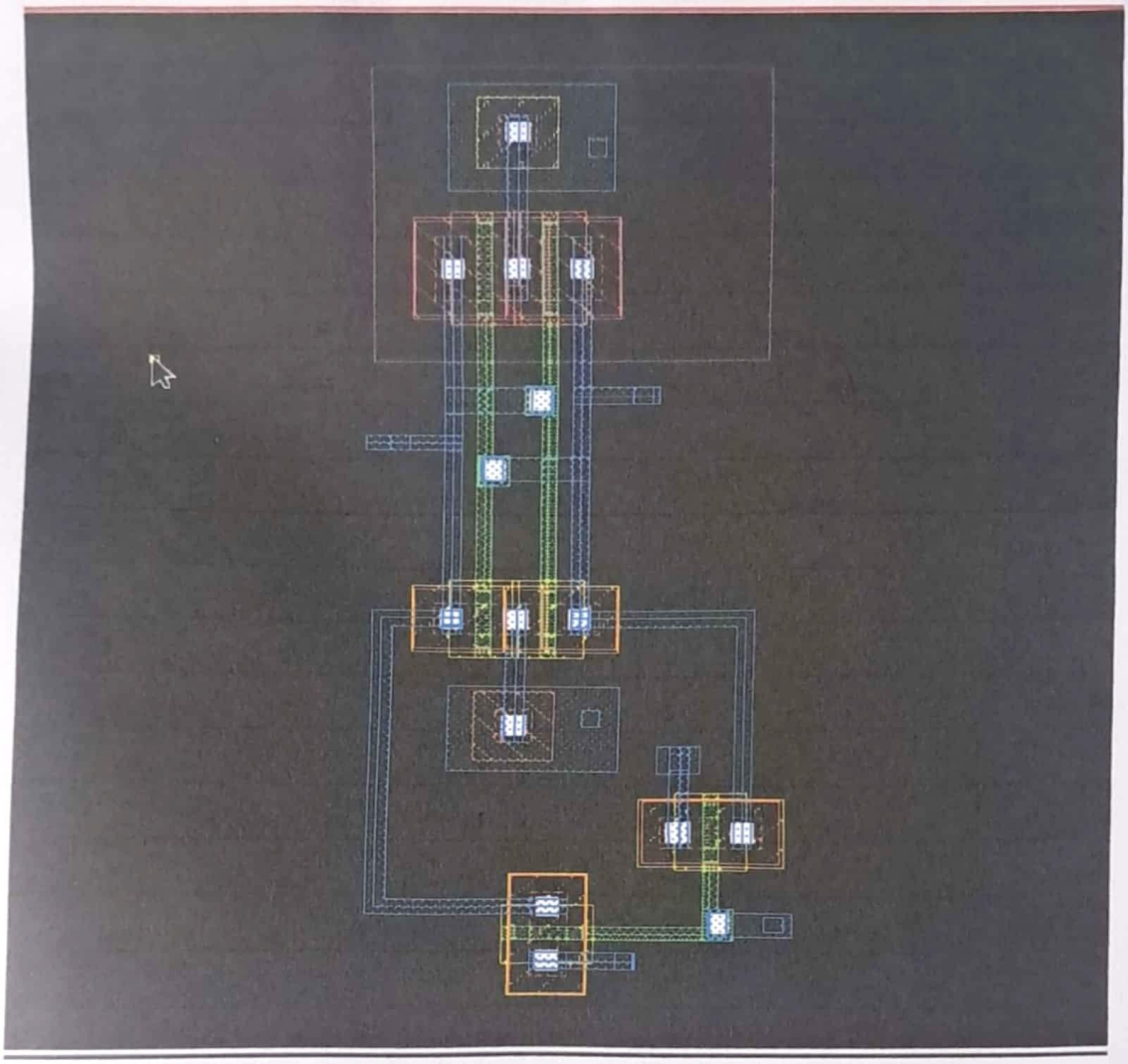


Figure 4.6: Layout of Conventional 6T SRAM

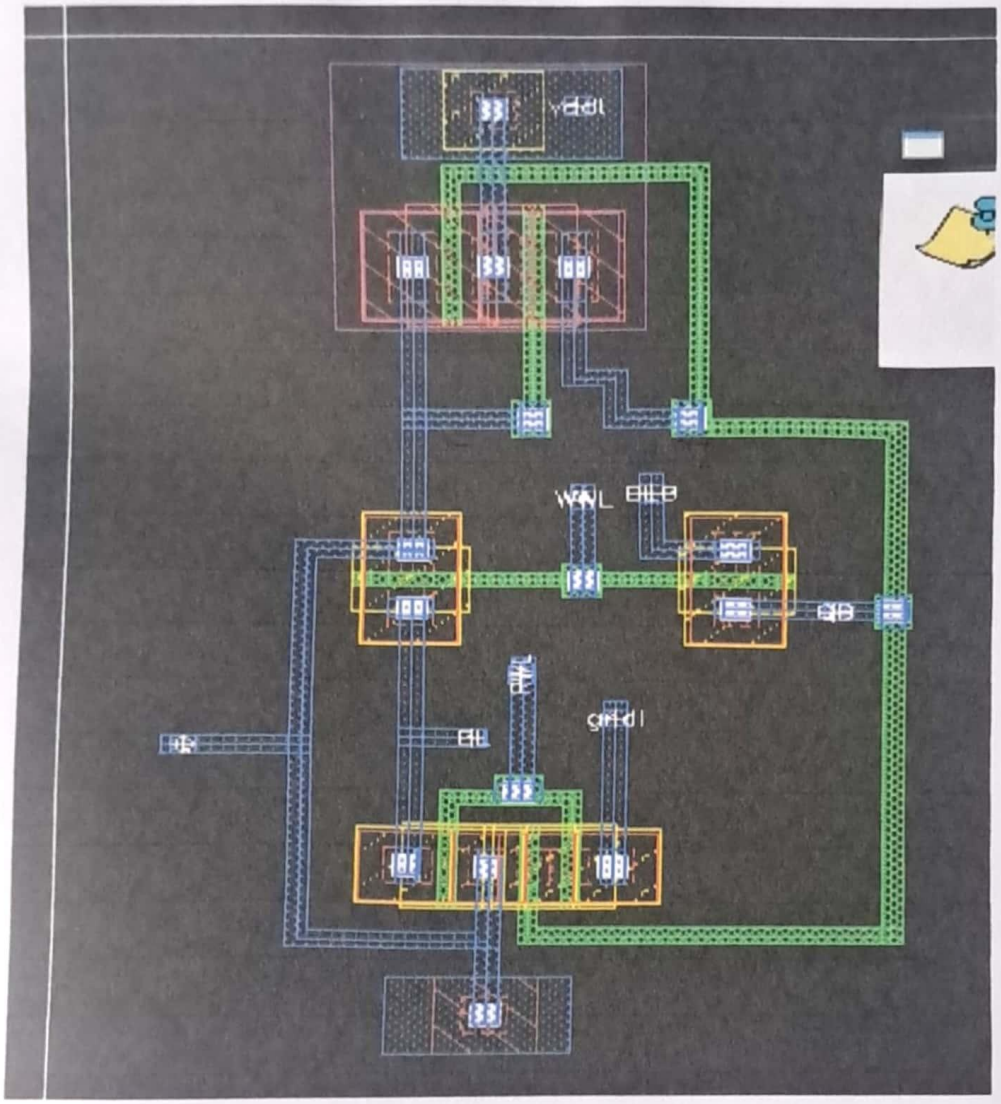


Figure 4.7: Layout of 7T SRAM

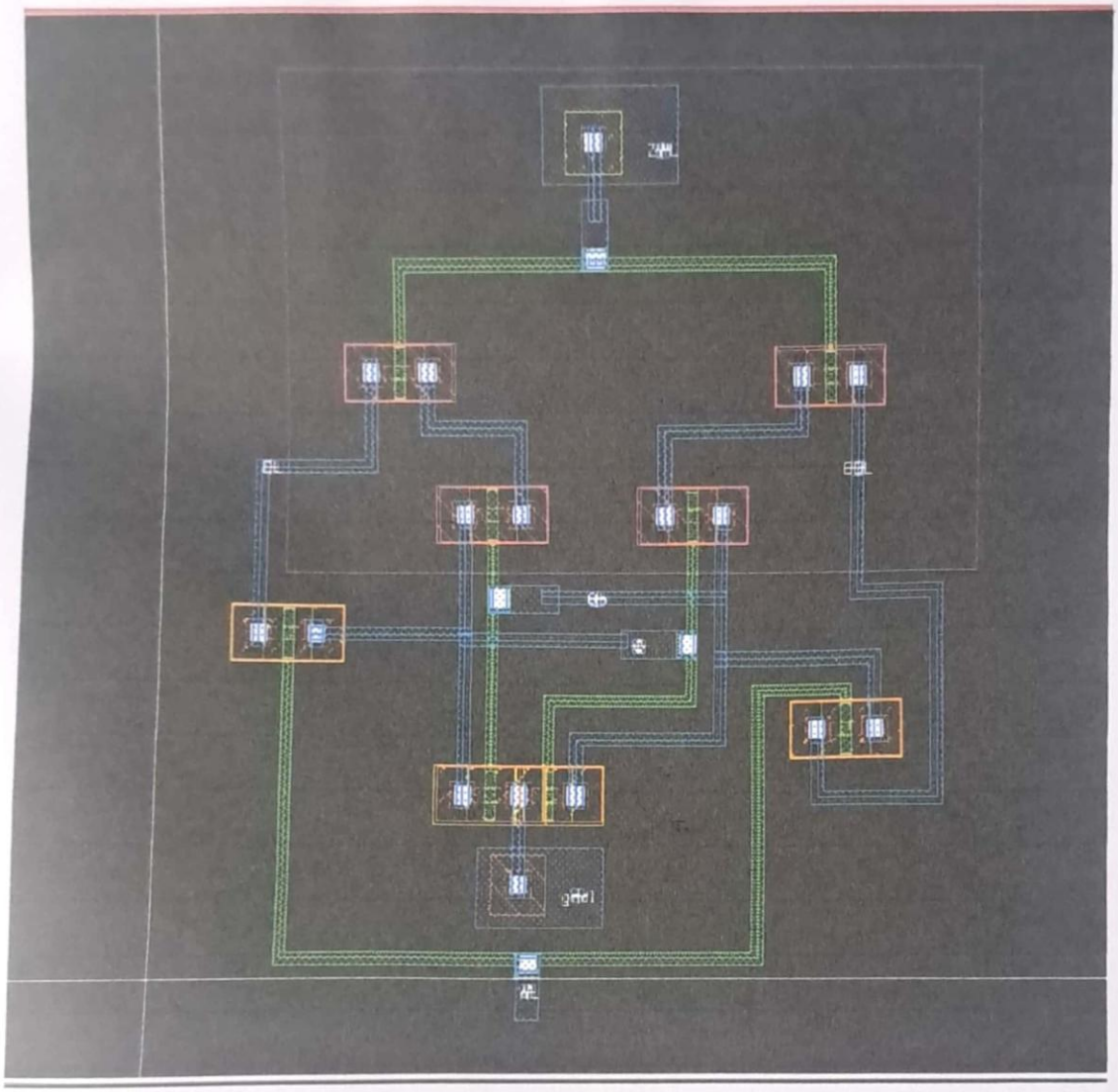


Figure 4.8: Layout of 8T SRAM

4.9 Layout of Proposed 9T SRAM

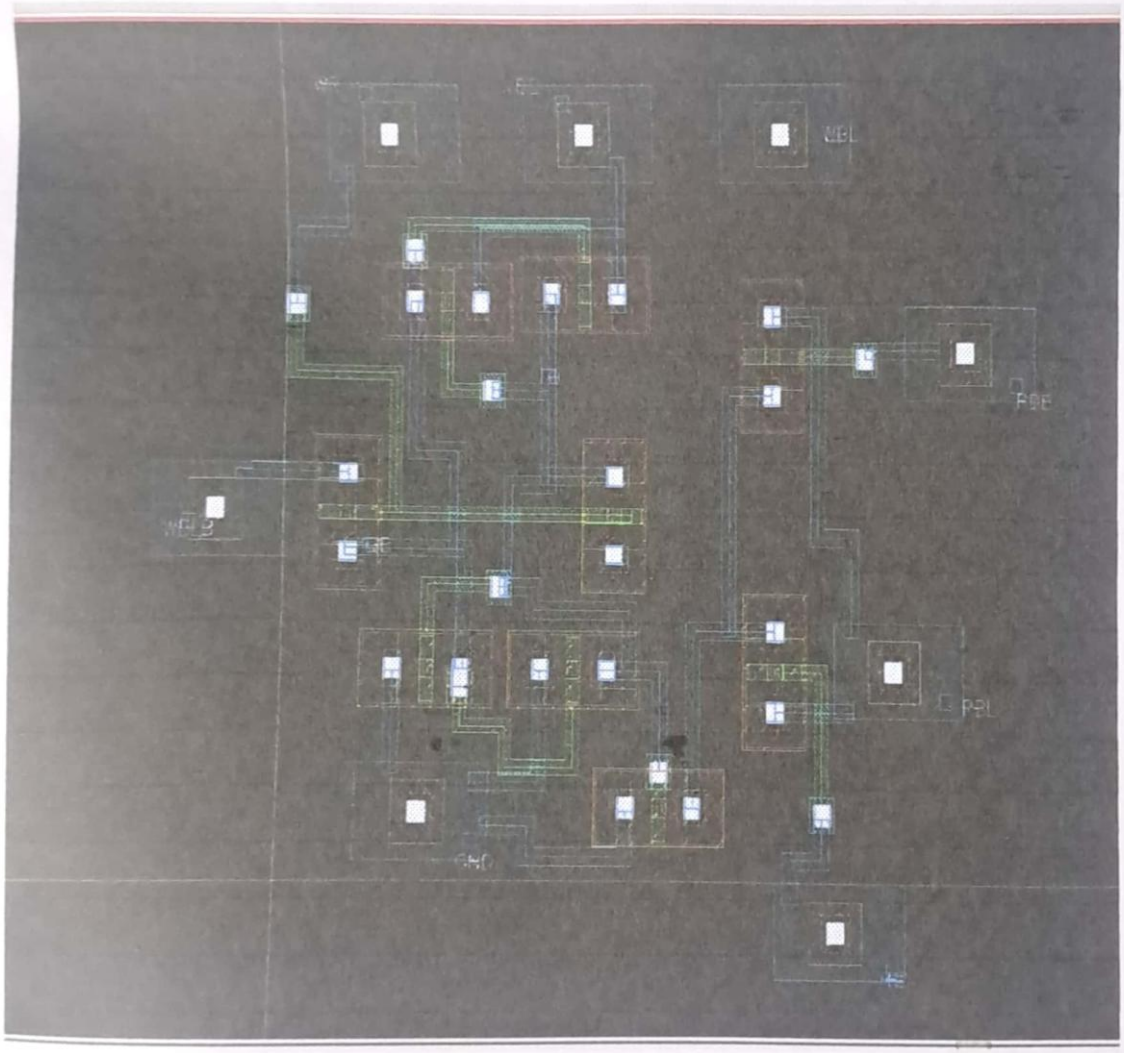


Figure 4.9: Proposed 9T SRAM

Chapter 5

Conclusion

5.1 Contribution of Proposed 9T SRAM Cell

SRAM Cells come in various varieties depending on the number of transistors. The proposed 9T SRAM Cell consists of 9 transistors and the circuit design is different from the traditional 9T cell. The results were obtained for 3 different CMOS technologies (22nm, 32nm, and 45nm) using the LTSpice circuit simulator. Read operation, average power consumption and propagation delay waveforms were observed In the LT Spice simulation. Hence, to summarize the acquired result:

- The principle purpose of lowering power consumption and enhancing the cell life has been achieved in the proposed cell. The total average power is improved by a vast margin of 90% which surpasses the conventional 6T and other cells.

- The use of extra transistors improved the cell performance considerably and reduced the leakage current. The proposed 9T SRAM showed the least amount of leakage current as opposed to conventional 6t, 9t & other topologies.

- The Power Delay Product is the indicator of cell efficiency which is the lowest in the proposed cell. So, the proposed 9T SRAM is high in efficiency and functional speed.

- The stability of the proposal cell is improved during read operation due to the addition of decoupled circuit. 9T SRAM cell would simultaneously reduce leakage power and enhance data stability.

5.2 Limitations of Proposed 9T SRAM Cell

•The proposed 9t SRAM has a larger area due to extra transistors which is a setback for the application in smaller devices and microprocessors.

• Given that, the transistors are not ideal and the design is not perfect some amount of delay is present in every cell model. The proposed 9t SRAM model doesn't have the lowest time delay but the 45nm gives a delay closer to the conventional 6T.

5.3 Future Scopes

As the world is developing rapidly, we must likewise advance our technologies, programs, and appliances to keep up. In recent times the demand for portable electronic devices with long battery life is at its peak. Some suggestions for future work using the proposed model:

• The most salient feature of the proposed 9T SRAM cell among other
the cell is its low power requirement and better performance. So, it can be integrated into portable handheld devices due to high data speed with no refresh needed.

• Hence, the cell can meet the demands of faster cache memory in microprocessors and can be used in phones, smart watches, GPS devices, music players, graphics cards, and other consumer electronics.

• It can also be embedded in medical devices, automobiles, industrial equipment, IoT devices, etc.

Further research and design modifications can be done with this model in order to improve

the speed and stability. To attain reduced area in layout design, circuit design modifications can be done. Moreover, Fin-FET and CNTFET models can be used in place of traditional MOSFETs to achieve area reduction and superior results in other parameters. Different low-power techniques can be applied to enhance performance for practical application and fabrication.

References

[1] Types of Computer Memory: RAM, ROM and Secondary Memory- https://www.seeedstudio.com/blog/2020/11/25/types-of-computer-memory-ram-rom-and-secondary-memory/

[2] International Technology Roadmap for Semiconductors. - http://www.evaluationengineering.com/index.php/solutions/ate/manufacturability-withembedded-infrastructure-ips.html.

[3]B.Cheng, S.Roy, G.Roy, A.Brown, and A.Asenov, "Impact of Random Dopant Fluctuation on Bulk CMOS 6-T SRAM Scaling" in Solid-State Device Research Conference,2006.

[4] Basic Electronics - MOSFET- https://www.tutorialspoint.com/basic_electronics/basic_electronics_mosfet.htm

[5] Digital Electronics: Memory Devices- https://www.brainkart.com/article/Important-Short-Questions-and-Answers--Digital-Electronics---Memory-Devices_12990/

[6] SRAM Circuit Design and Operation (Read-Write) | Working of SRAM- https://digitalthinkerhelp.com/sram-circuit-design-and-operation-read-write-working-of-sram/

[7] Overcoming Design and Process Challenges in Next-Generation SRAM Cell Architectures
Published by Benjamin Vincent on March 8, 2021

[8] G.E.Moore, "Cramming more components onto integrated circuits, "Electronics, vol. 38, no.8, April 1965.

[9] K.Zhang, (Ed.), "Embedded memories for nano-scale VLSI"(Vol.2). New York: Springer. (2009).

[10] Power Consumption (Components of power consumption)- https://semiengineering.com/knowledge_centers/low-power/low-power-design/power-consumption/

[11]R.K.Krishnamurthy, A.Alvandpour, V.De, and S.Borkar, "High-performance and low-power challenges for sub-70 nm microprocessor circuits, "Proc.IEEE Custom Integrated Circuit Conf.,(pp.125-128,2002)

[12] T.Azam,B.Cheng,&D.R.Cumming,(2010,March),"Variability resilient low-power 7T-SRAM design for nano-scaled technologies ". 2010 IEEE 11th International Symposium on Quality Electronic Design (ISQED), (pp.9-14)

[13] Shah M. Jahinuzzaman, "Modeling and Mitigation of Soft Errors in Nanoscale SRAMs.' Waterloo, Ontario, Canada, 2008, pp: 25-44

[14]Jawar Singh, J. Mathew, S. Mohanty, "A subthreshold single-ended I/O SRAM cell design for nanometer CMOS technologies."2008 IEEE International SOC Conference,pp:243-246

[15] Ezeogu Chinonso Apollos, "Performance Analysis of 6T and 9T SRAM."International Journal of Engineering Trends and Technology (IJETT) – Volume 67 Issue 4 - April 2019

[16] Mahdi Tavazoei and Farhad Razaghian, " A SINGLE-ENDED AND BIT-INTERLEAVING 7T SRAM CELL IN SUB-THRESHOLD REGION WITH A SMALL AREA CONSUMPTION." International Journal of Electronic Design and Test (JEDT) Vol.1 No.3, pp: 3-4

[17] Nahid Rahman, B. P. Singh, "Design of Low Power Sram Memory Using 8t Sram Cell." International Journal of Recent Technology and Engineering (IJRTE), ISSN: 2277-3878, Volume-2 Issue-1, March 2013

[18] Abhinandan Goswami,Amit Singh Rajput,Nikhil Saxena, "A DOUBLE-ENDED WRITE SINGLE-ENDED READ DECOUPLED 9T SRAM CELL WITH FASTER READ SPEED AND IMPROVED READ STABILITY".Vol.4., Issue.6., 2016 Nov-Dec

[19] LTSpice User Guide- http://www.linear.com/designtools/software/(1-800-4-LINEAR)

[20] Predictive Technology Model (PTM)- http://ptm.asu.edu/latest.html
[21] Cadence User Guide - http://www.cadence.com/content/cadence-www/global/en_US/home/tools/ic-package-design-and-analysis.html

[22] Shikha Saun and Hemant Kumar, " Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization.", 2019 IOP Conf. Ser.: